FIG. 1

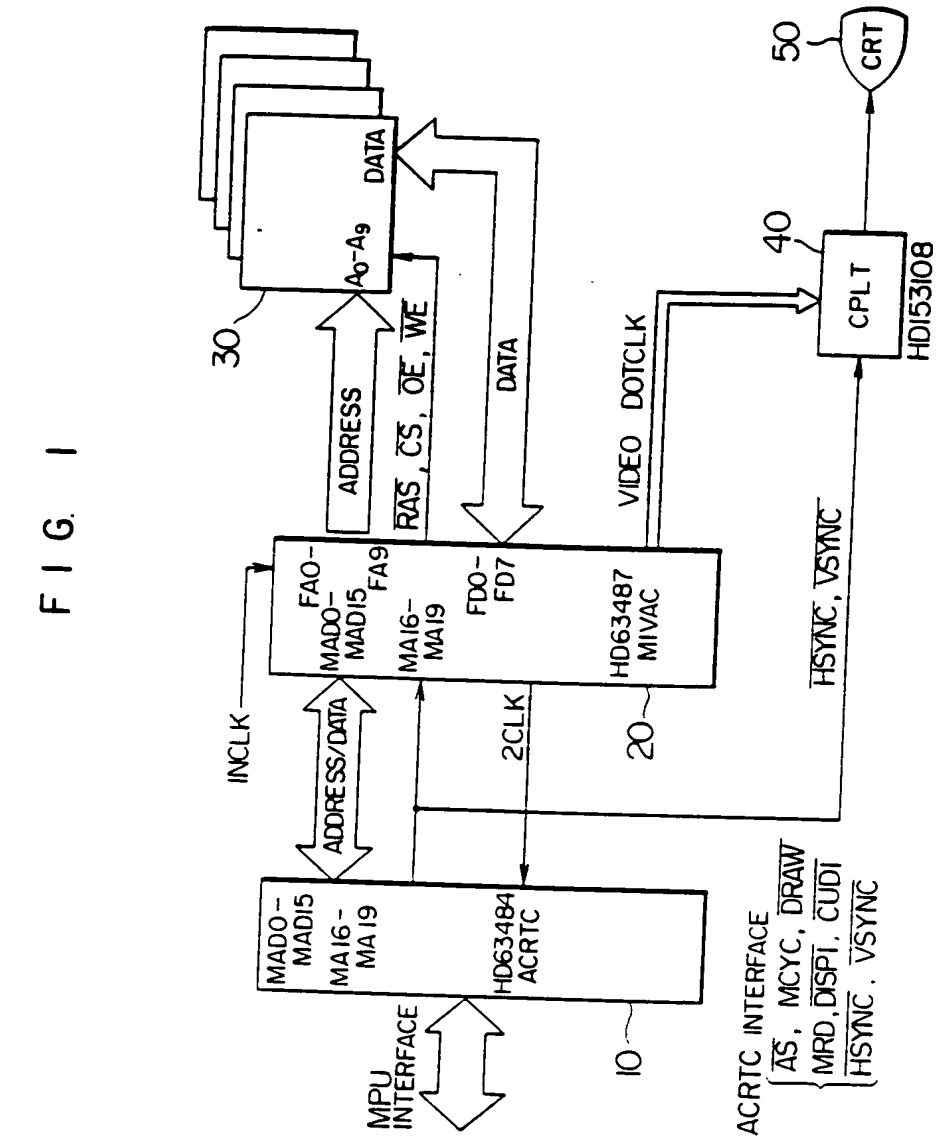

50
CRT
40
CPLT
HD153108
30
DATA
A0-A9
ADDRESS
RAS, CS, OE, WE
DATA
VIDEO DOTCLK
FA0-FA9
MA0-MA15
MA16-MA19
FD0-FD7
HD63487 MIVAC
20
INCLK
ADDRESS/DATA
2CLK
HSYNC, VSYNC
MA0-MA15
MA16-MA19
HD63484 ACRTC
10
MPU INTERFACE
ACRTC INTERFACE
AS, MCYC, DRAW
MRD, DSPI, CUDI
HSYNC, VSYNC

FIG. 2

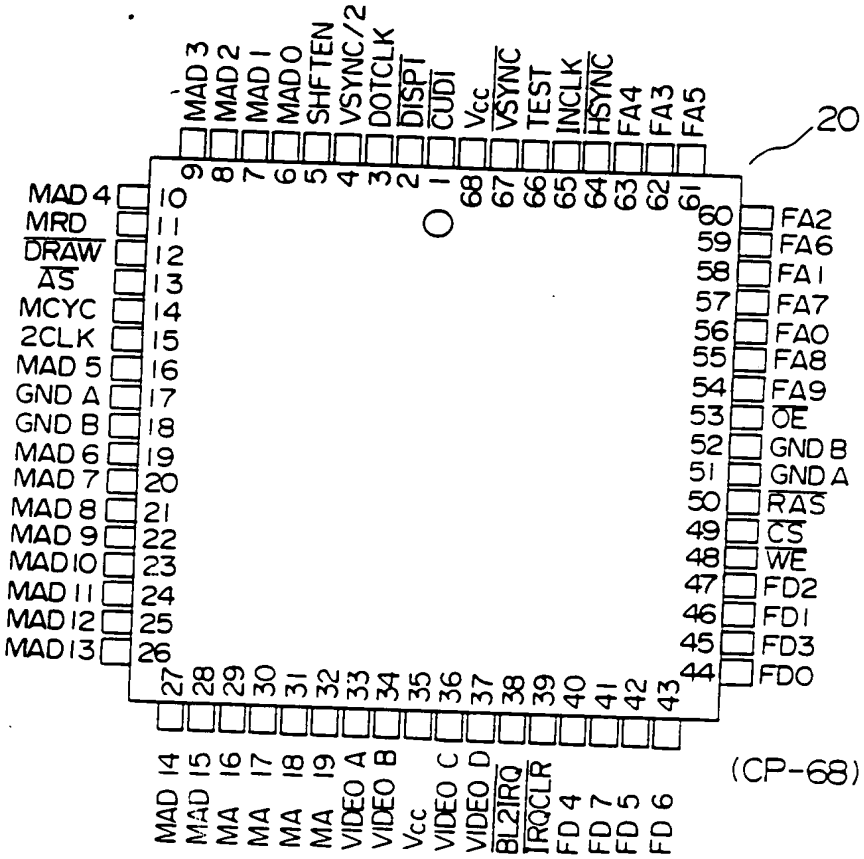

20
MAD 3
MAD 2
MAD 1
MAD 0
SHFTEN
VSYNC/2
DOTCLK
DISPT
CUDI
Vcc
VSYNC
TEST
INCLK
HSYNC
FA4
FA3
FA5
MAD 4
MRD
DRAW
AS
MCYC
2CLK
MAD 5
GND A
GND B
MAD 6
MAD 7
MAD 8
MAD 9
MAD 10
MAD 11
MAD 12
MAD 13
FA2
FA6
FA1
FA7
FA0
FA8
FA9
OE
GND B
GND A
RAS
CS
WE
FD2
FD1
FD3
FD0
MAD 14
MAD 15
MA 16
MA 17
MA 18
MA 19
VIDEO A
VIDEO B
Vcc
VIDEO C
VIDEO D
BL2IRQ
IRQCLR
FD 4
FD 7
FD 5
FD 6
(CP-68)

FIG. 3a

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
POWER SUPPLY	35,68	Vcc	—	+5V IS SUPPLIED.
	17,18 51,52	Vcc	—	GND IS CONNECTED.
OPERATION CONTROL SIGNAL	65	INCLK	INPUT	BASIC CLOCK OF MIVAC IS INPUTTED.
	66	TEST	INPUT	MIVAC OPERATION IS TESTED. SET THIS TERMINAL TO "LOW" LEVEL.
ACRTC INTERFACE SIGNAL	15	2CLK	OUTPUT	2CLK SIGNAL IS SUPPIED TO ACRTC. THIS SIGNAL IS ASYMMETRIC. NAMELY. HAS DIFFERENT CYCLE LENGTHS IN THE FIRST HALF AND SECOND HALF OF A MEMORY CYCLE
	14	MCYC	INPUT	MCYC SIGNAL FROM ACRTC IS INPUTTED. MCYC INDICATES "LOW" AND "HIGH" LEVELS WHEN ACRTC IS IN ADDRESS AND DATA CYCLES, RESPECTIVELY.
	12	$\overline{\text{DRAW}}$	INPUT	$\overline{\text{DRAW}}$ SIGNAL FROM ACRTC IS INPUTTED. $\overline{\text{DRAW}}$ INDICATES WHETHER OR NOT ACRTC IS IN THE DRAW CYCLE. $\overline{\text{DRAW}}$ IS "LOW" LEVEL IN THE DRAW CYCLE AND IS "HIGH" LEVEL IN THE OTHER CYCLES.
	11	MRD	INPUT	MRD SIGNAL FROM ACRTC IS INPUTTED. MRD CONTROLS DATA TRANSFER DIRECTION BETWEEN FRAME BUFFER AND ACRTC. WHEN DATA IS READ FROM FRAME BUFFER, "HIGH" LEVEL IS INPUTTED. WHEN DATA IS WRITTEN IN FRAME BUFFER, "LOW" LEVEL IS INPUTTED.
	13	$\overline{\text{AS}}$	INPUT	$\overline{\text{AS}}$ SIGNAL IS INPUTTED FROM ACRTC $\overline{\text{AS}}$ INDICATES PRESENCE OR ABSENCE OF MEMORY ACCESS.
	64	$\overline{\text{HSYNC}}$	INPUT	HSYNC SIGNAL IS INPUTTED FROM ACRTC. UNDER CONDITIONS OF $\overline{\text{HSYNC}}$ = "LOW" AND $\overline{\text{DRAW}}$ = "HIGH", IF AS PULSE IS RECEIVED, $\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH OPERATION IS CARRIED OUT.
	67	$\overline{\text{VSYNC}}$	INPUT	$\overline{\text{VSYNC}}$ SIGNAL IS INPUTTED FROM ACRTC. RECEIVED $\overline{\text{VSYNC}}$ IS DIVIDED BY TWO SO AS TO OUTPUTTED AS VSYNC/2 SIGNAL AND IS ALSO USED TO CONTROL MULTIPLEXER OF VIDEO OUTPUT.
	2	$\overline{\text{DISP 1}}$	INPUT	$\overline{\text{DISP 1}}$ SIGNAL IS INPUTTED FROM ACRTC. $\overline{\text{DISP 1}}$ INDICATES SCREEN DISPLAY PERIOD. ORDINARILY, SET "1" TO DISPLAY SIGNAL CONTROL (DSC) BIT OF ACRTC.
	1	$\overline{\text{CUD 1}}$	INPUT	$\overline{\text{CUD 1}}$ SIGNAL IS INPUTTED FROM ACRTIC. $\overline{\text{CUD 1}}$ IS LOADED WITH "LOW" LEVEL DURING GRAPHIC CURSOR DISPLAY PERIOD.
	6–10 16 19–28	MAD0 –MAD 15	INPUT/OUTPUT	MOD0–MAD 15 OF ACRTC ARE INPUTTED. THESE SIGNALS ARE USED AS FRAME BUFFER ACCESS ADDRESS IN ADDRESS CYCLE FOR MCYC = "LOW". AS DATA INPUT/OUTPUT FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER IN DATA TRANSFER CYCLE FOR MCYC = "HIGH".
	29–32	MA16– MA19	INPUT	FRAME BUFFER ACCESS ADDRESS MA16 – MA19 IS INPUTTED FROM ACRTC.

FIG. 3b

ITEM	TERMINAL NO.	TERMINAL NAME	INPUT/OUTPUT	FUNCTION
FRAME BUFFER INTERFACE SIGNAL	50	$\overline{RAS}$	OUTPUT	$\overline{RAS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	49	$\overline{CS}$	OUTPUT	$\overline{CS}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	48	$\overline{WE}$	OUTPUT	$\overline{WE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	53	$\overline{OE}$	OUTPUT	$\overline{OE}$ TIMING SIGNAL IS OUTPUTTED FOR DRAM.
	56,58 60,62 63,61 59,57 55,54	FA0 - FA 9	OUTPUT	MULTIPLEX ADDRESS IS OUTPUTTED FOR DRAM. ADDRESS TO BE MULTIPLEXED VARIES DEPENDING ON VCF 0 - VCF 3 AND VMD 0 ATTRIBUTE CODES.
	44,46 47,45 40,42 43,41	FD0 - FD7	INPUT/OUTPUT	FD IS 8-BIT INPUT/OUTPUT SIGNAL FOR DATA TRANSFER BETWEEN ACRTC AND FRAME BUFFER AND FOR FETCHING DISPLAY DATA READ FROM FRAME BUFFER. IN A CASE OF ONE MEMORY CHIP, FD 0 - FD 3 ARE USED, WHEREAS IN A CASE OF TWO FOUR MEMORY CHIPS, FD 0 - FD 7 ARE USED.
CRT DISPLAY INTERFACE SIGNAL	3	DOTCLK	OUTPUT	DOTCLK SIGNAL IS DELIVERED BY DIVIDING INCLK SIGNAL AS BASIC INPUT SIGNAL OF MIVAC BY 1, 2 OR 4. DIVISION RATIO IS SET DEPENDING ON VCF 0 - VCF 3 OF ATTRIBUTE CODE.
	33, 34 36, 37	VIDEO A -VIDEO D	OUTPUT	VIDEO A-D SIGNAL IS 4-BIT OUTPUT SIGNAL WHICH IS OBTAINED BY CONVERTING DISPLAY DATA FROM PARALLEL SIGNAL INTO SERIAL SIGNAL BY SHIFT REGISTER OF MIVAC AND WHICH IS DELIVERED DURING DISPLAY PERIOD INDICATED BY SHFTEN OUTPUT. 4-BIT VIDEO SIGNAL IS DETERMINED BY ATTRIBUTE CODE VCF 0 - VCF 3.
	5	SHFTEN	OUTPUT	SHFTEN INDICATES DISPLAY PERIOD OF VIDEO SIGNAL AND IS SET TO "HIGH" LEVEL DURING DISPLAY PERIOD. IN SINGLE ACCESS, $\overline{DISP1}$ FROM ACRTC IS ELONGATED BACKWARD BY ONE CYCLE, AND IN DUAL ACCESS, $\overline{DISP1}$ IS ELONGATED BACKWARD BY TWO CYCLES SO AS TO PRODUCE THIS SIGNAL.
	4	VSYNC/2	OUTPUT	VSYNC/2 SIGNAL IS INPUTTED TO ACRTC. $\overline{VSYNC}$ IS DIVIDED BY TWO FOR PRODUCING THIS SIGNAL.
OTHERS	38	$\overline{BL2IRQ}$	OUTPUT	$\overline{BL2IRQ}$ IS SET BY BLINK2 (MA19) INPUTTED IN ATTRIBUTE CYCLE. DURING ATTRIBUTE CYCLE, WHEN BLINK 2 IS AT "HIGH" LEVEL, $\overline{BL2IRQ}$ IS SET TO "LOW" LEVEL.
	39	$\overline{IRQCLR}$	INPUT	$\overline{IRQCLR}$ SIGNAL IS USED TO CLEAR $\overline{BL2IRQ}$ SIGNAL. WHEN "LOW" IS INPUTTED TO $\overline{IRQCLR}$, $\overline{BL2IRQ}$ IS CLEARED TO "HIGH" LEVEL.

FIG. 4

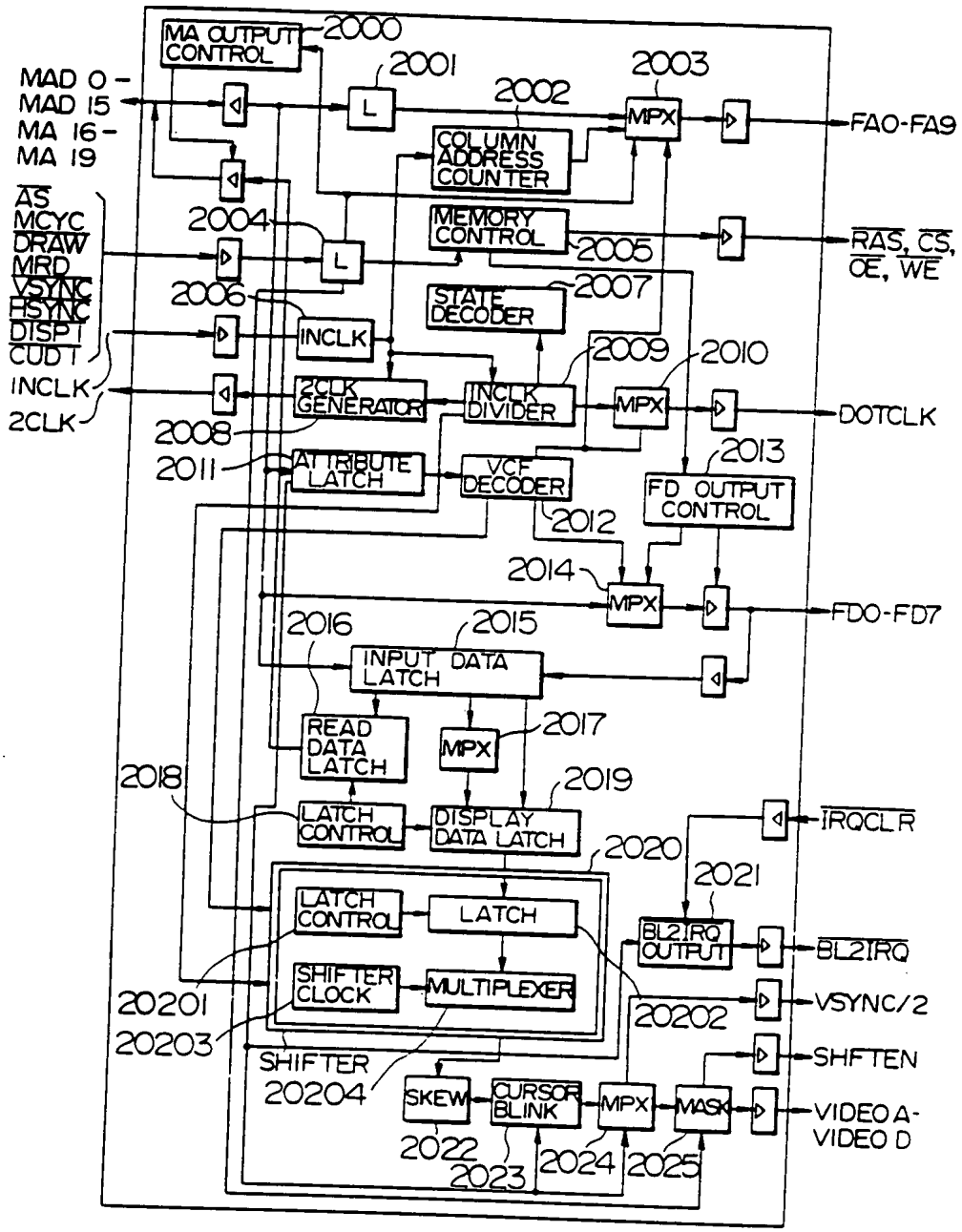

MA OUTPUT CONTROL
2000
2001
2002
2003
MAD 0 - MAD 15
MA 16 - MA 19
L
MPX
FA0-FA9
COLUMN ADDRESS COUNTER
AS
MCYC
DRAW
MRD
VSYNC
HSYNC
DISPT
CUDT
INCLK
2CLK
2004
MEMORY CONTROL
2005
RAS, CS, OE, WE
2006
STATE DECODER
2007
INCLK
2CLK GENERATOR
INCLK DIVIDER
2009
2010
DOTCLK
2008
2011
ATTRIBUTE LATCH
VCF DECODER
2012
FD OUTPUT CONTROL
2013
2014
FD0-FD7
2016
2015
INPUT DATA LATCH
READ DATA LATCH
2017
2018
2019
LATCH CONTROL
DISPLAY DATA LATCH
IRQCLR
2020
2021
LATCH
BL2IRQ OUTPUT
BL2IRQ
SHIFTER CLOCK
MULTIPLEXER
VSYNC/2
20201
20202
20203
SHIFTER
SHFTEN
20204
SKEW
CURSOR BLINK
MASK
VIDEO A-VIDEO D
2022
2023
2024
2025

FIG. 5a

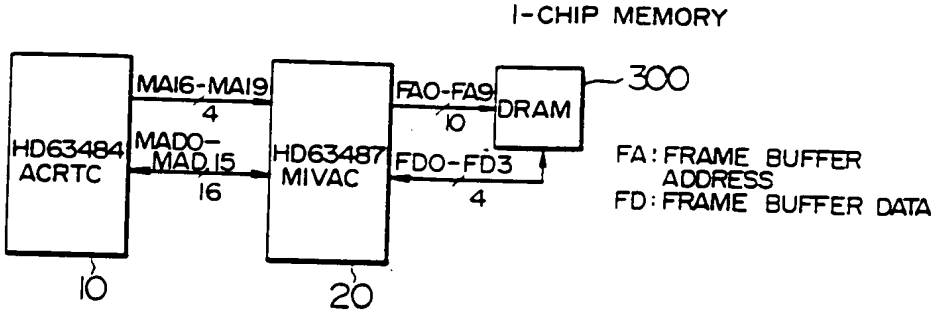


FIG. 5b

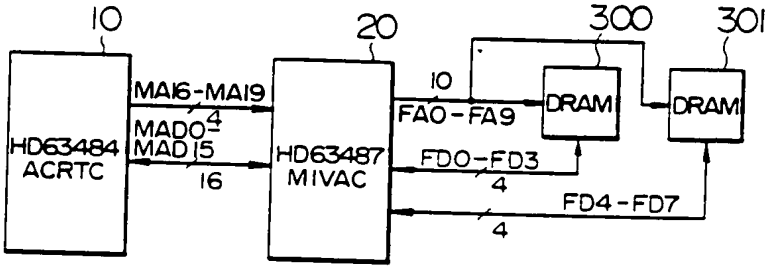


FIG. 5c

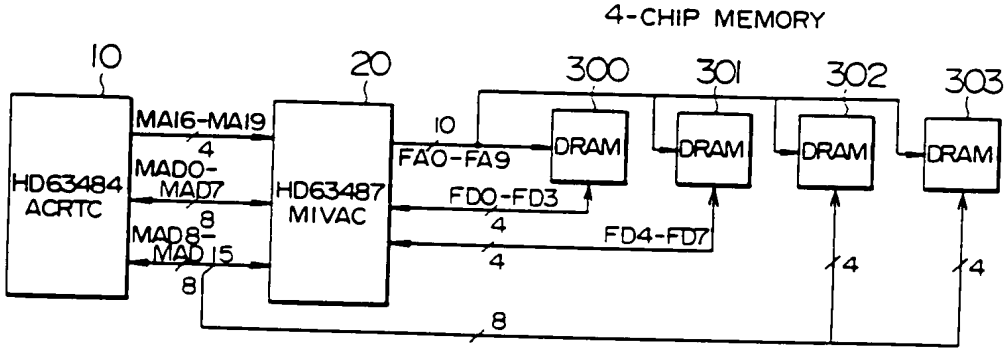


FIG. 6

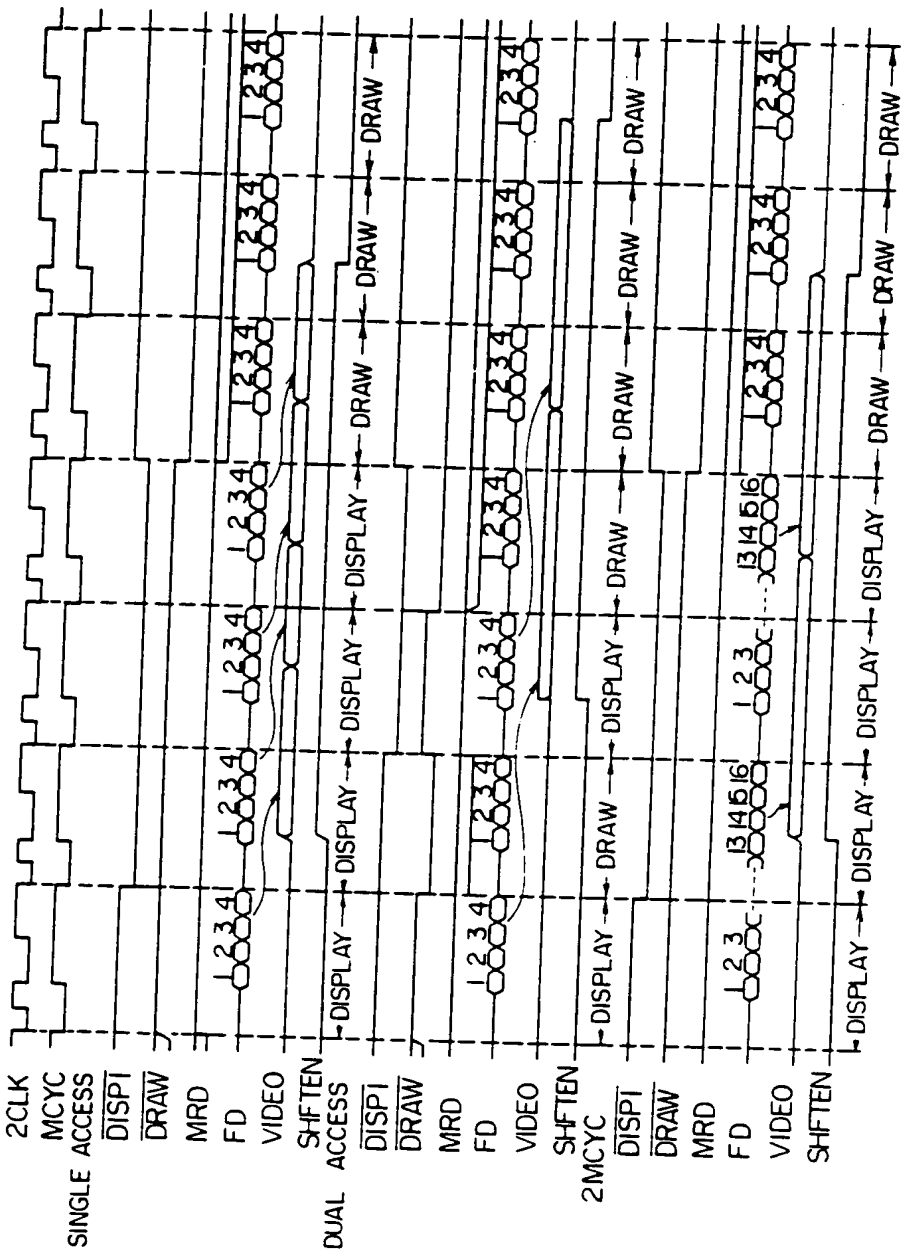

2CLK
MCYC
SINGLE ACCESS
DISPI
DRAW
MRD
FD
VIDEO
SHFTEN
DUAL ACCESS
DISPI
DRAW
MRD
FD
VIDEO
SHFTEN
2MCYC
DISPI
DRAW
MRD
FD
VIDEO
SHFTEN
DISPLAY
DRAW

FIG. 7

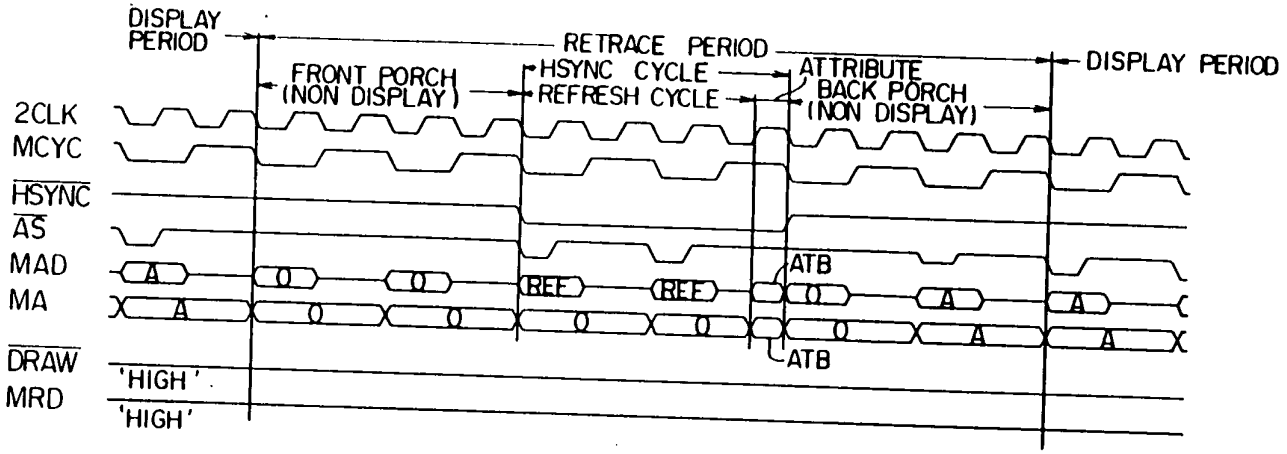


FIG. 11

CUR 1	CUR 0	CURSOR DISPLAY COLOR
0	0	BLACK (VIDEO A - VIDEO D = 0)
0	1	WHITE (VIDEO A - VIDEO D = 1)
1	0	COLOR REVERSION FOR EACH BIT OF VIDEO A - VIDEO D
1	1	COLOR REVERSION FOR EACH BIT OF VIDEO A-VIDEO C (VIDEO D IS KEPT UNCHANGED)

FIG. 8

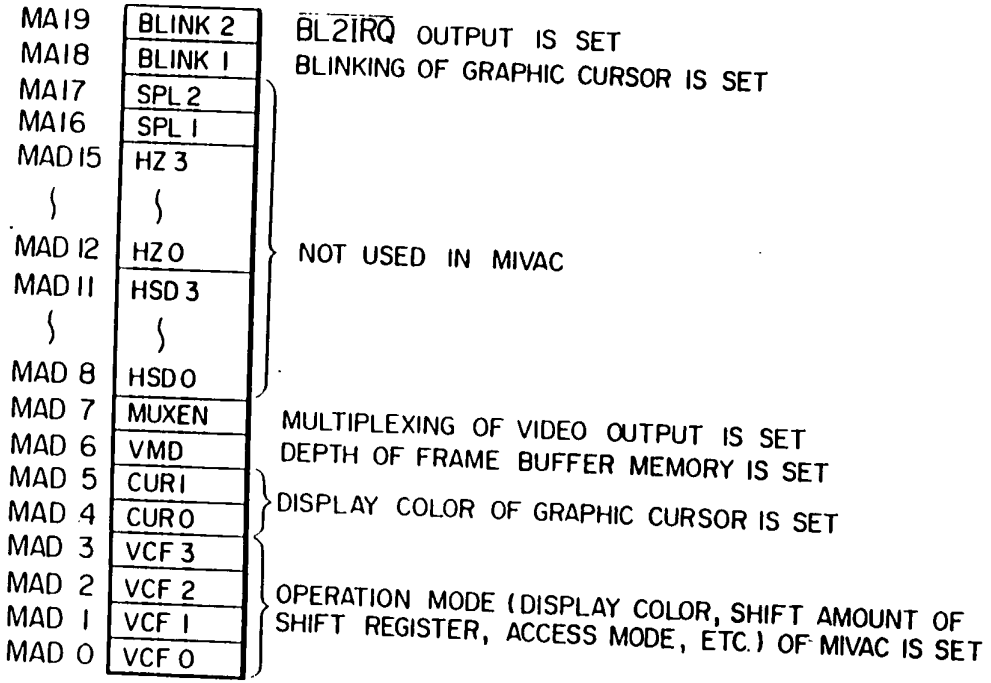


FIG. 9

MODE	CRT SCREEN LAYOUT EXAMPLE (DOTS X RASTER)	MAXIMUM FRAME BUFFER CAPACITY (BYTES)	ACRTC OPERATION FREQUENCY (MHz)	MEMORY ACCESS SPEED	HIGH-SPEED DRAWING	NUMBER OF MEMORIES	COLOR/GRADATION	SHIFT AMOUNT (BITS)	MAXIMUM DOT CLOCK FREQ. (MHz)
0	640×200, 350, 400, 480	512K/128K	4.13	480ns/4ACCESSES	—	1		16	33
1	640×200, 480×240, 320×200, 240						4	8	16.5
2	320×200, 240 266×192						16	4	8.25
3	640×200, 350, 400, 480	1M/256K				2	4	16	33
4	640×200, 480×240, 320×200, 240						16	8	16.5
5	640×200, 350, 400, 480	2M/512K				4			
6	640×200, 480×240, 320×200, 240	512K/128K			O	1		16	33
7	320×200, 240 256×192,						4		16.5
8	640×200, 350, 400, 480	1M/256K						8	8.25
9	640×200, 480×240, 320×200, 240					2		32	33
A	320×200, 240 256×192						4	16	16.5
B	640×200, 350, 400, 480	2M/512K					16	8	8.25
C	640×200, 480×240, 320×200, 240					4	4	32	33
D	640×200, 350, 400, 480	512K/128K					16	16	16.5
E	640×200, 480×240, 320×200, 240			960ns/16ACCESSES	—	1	4	32	33
F	640×200, 350, 400, 480	1M/256K					16	16	16.5
						2		32	33

FIG. 10

MODE	DOT CLOCK FREQUENCY
0, 3, 5, 8 B, D, F	33MHz ~ 11MHz
1, 4, 6, 9 C, E	16.5MHz ~ 5.5MHz
2, 7, A	8.25MHz ~ 2.75MHz

FIG. 12

VMD	MEMORY CHIP EMPLOYED
0	256K × 4BIT DRAM
1	1M × 4 BIT DRAM

FIG. 13

MUXEN	VSYNC/2	VIDEO A	VIDEO B
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

FIG. 14

BLINK 1	GRAPHIC CURSOR DISPLAY
0	NOT DISPLAYED
1	DISPLAYED

FIG. 15a

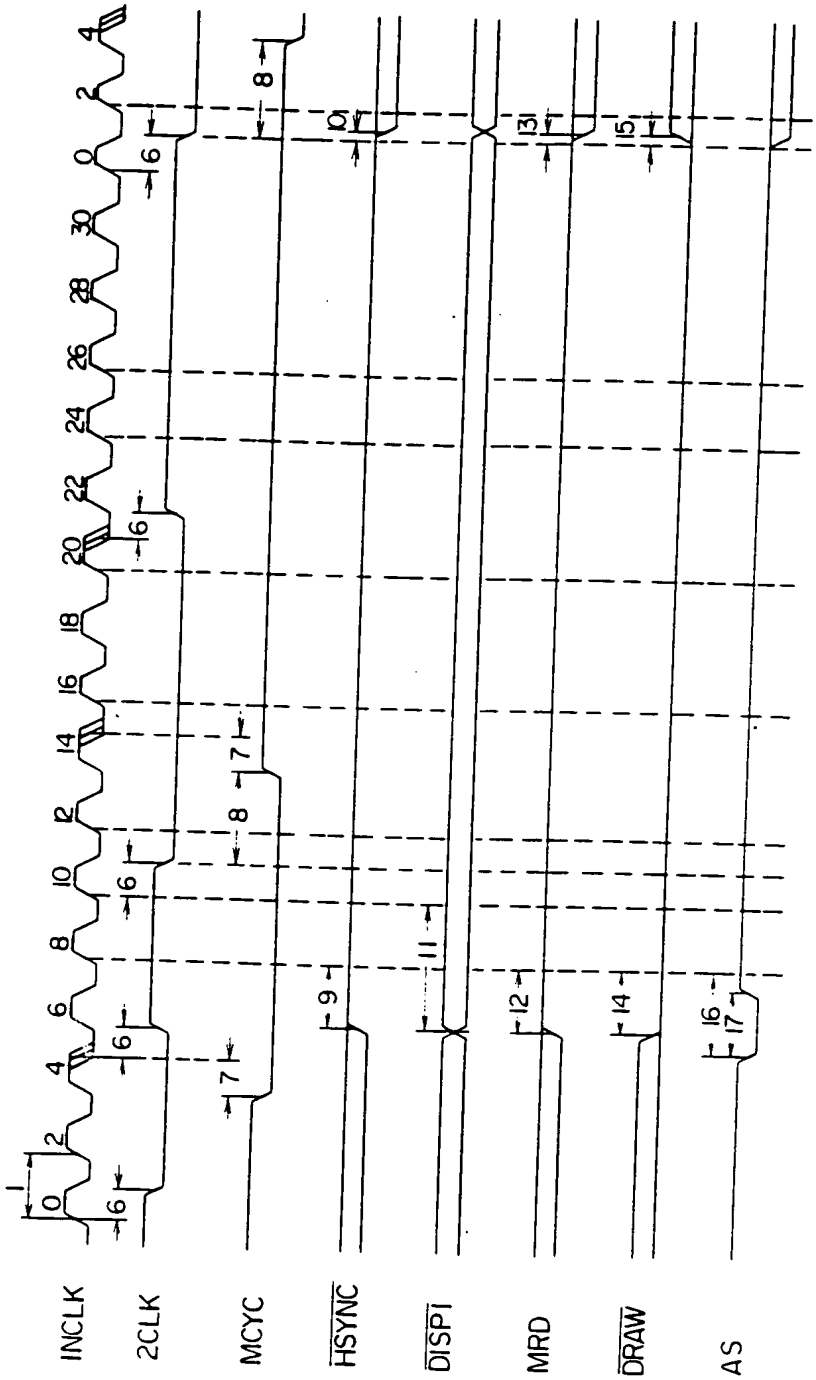


FIG. 15b

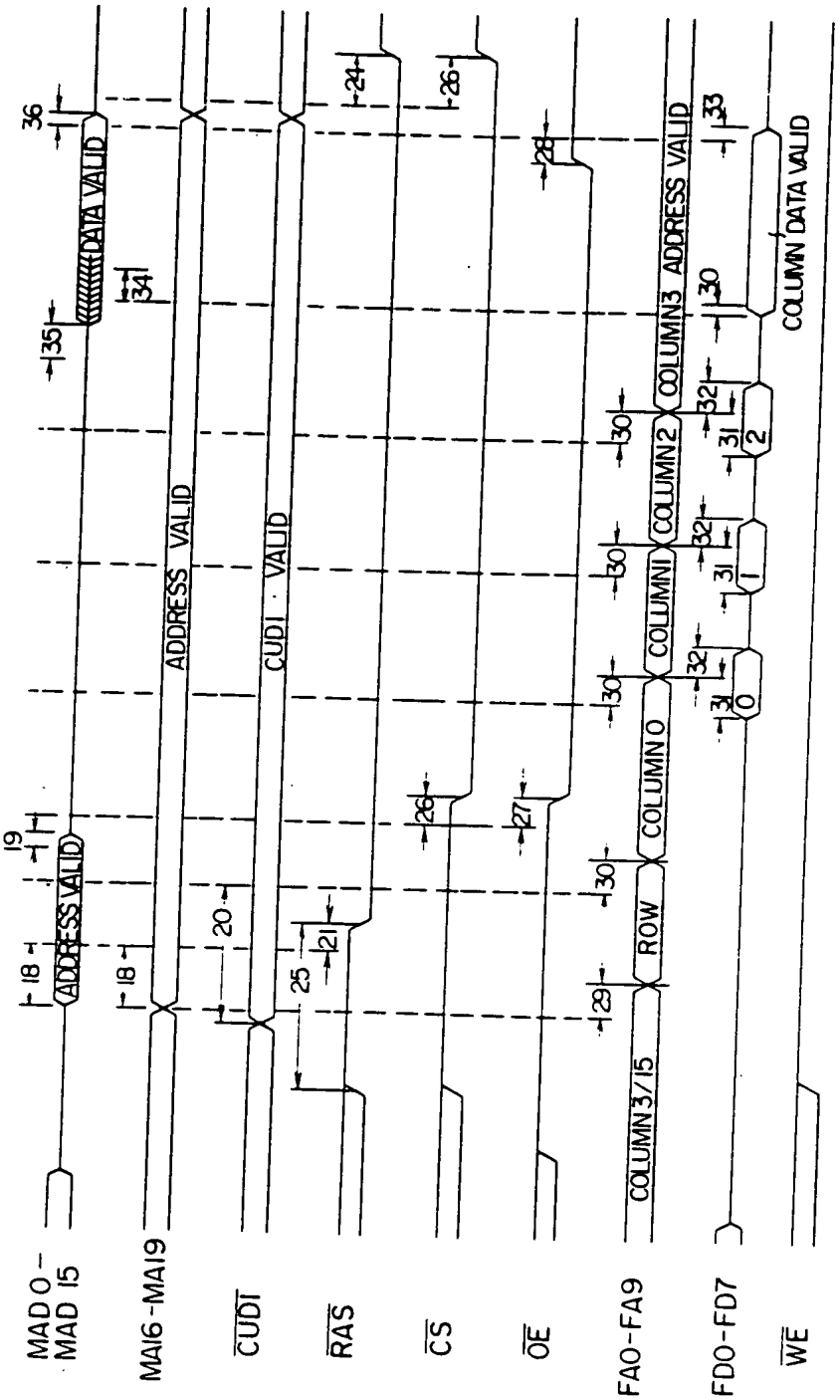

MAD 0 - MAD 15
MA16 - MA19
CUDI
RAS
CS
OE
FA0 - FA9
FD0 - FD7
WE
ADDRESS VALID
DATA VALID
CUDI VALID
ROW
COLUMN 3/15
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3 ADDRESS VALID
COLUMN DATA VALID
0
1
2
18
19
20
21
24
25
26
27
28
29
30
31
32
33
34
35
36

FIG. 16a

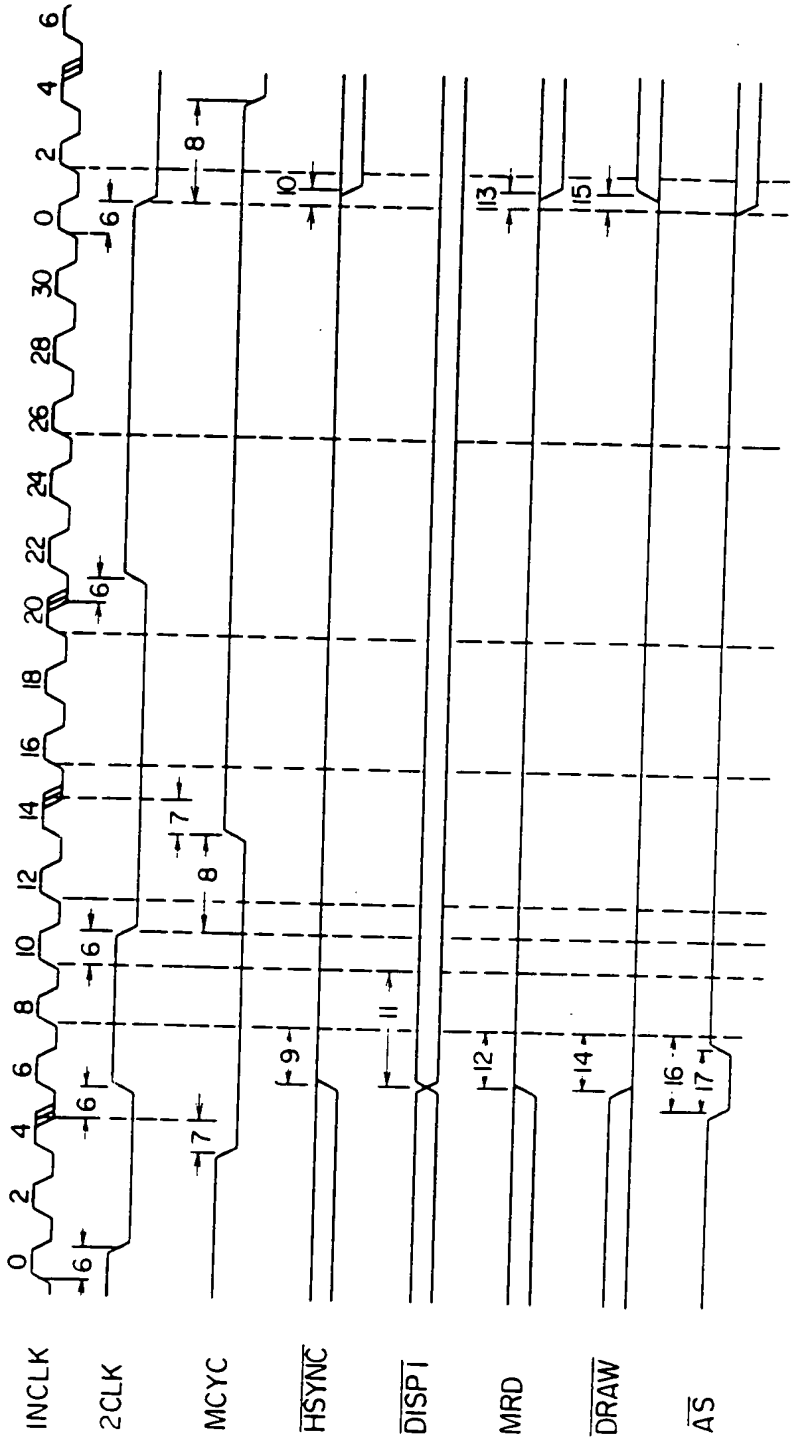

INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
0
2
4
6
6
6
6
6
7
7
8
8
10
11
9
12
14
16
17
113
115

FIG 16b

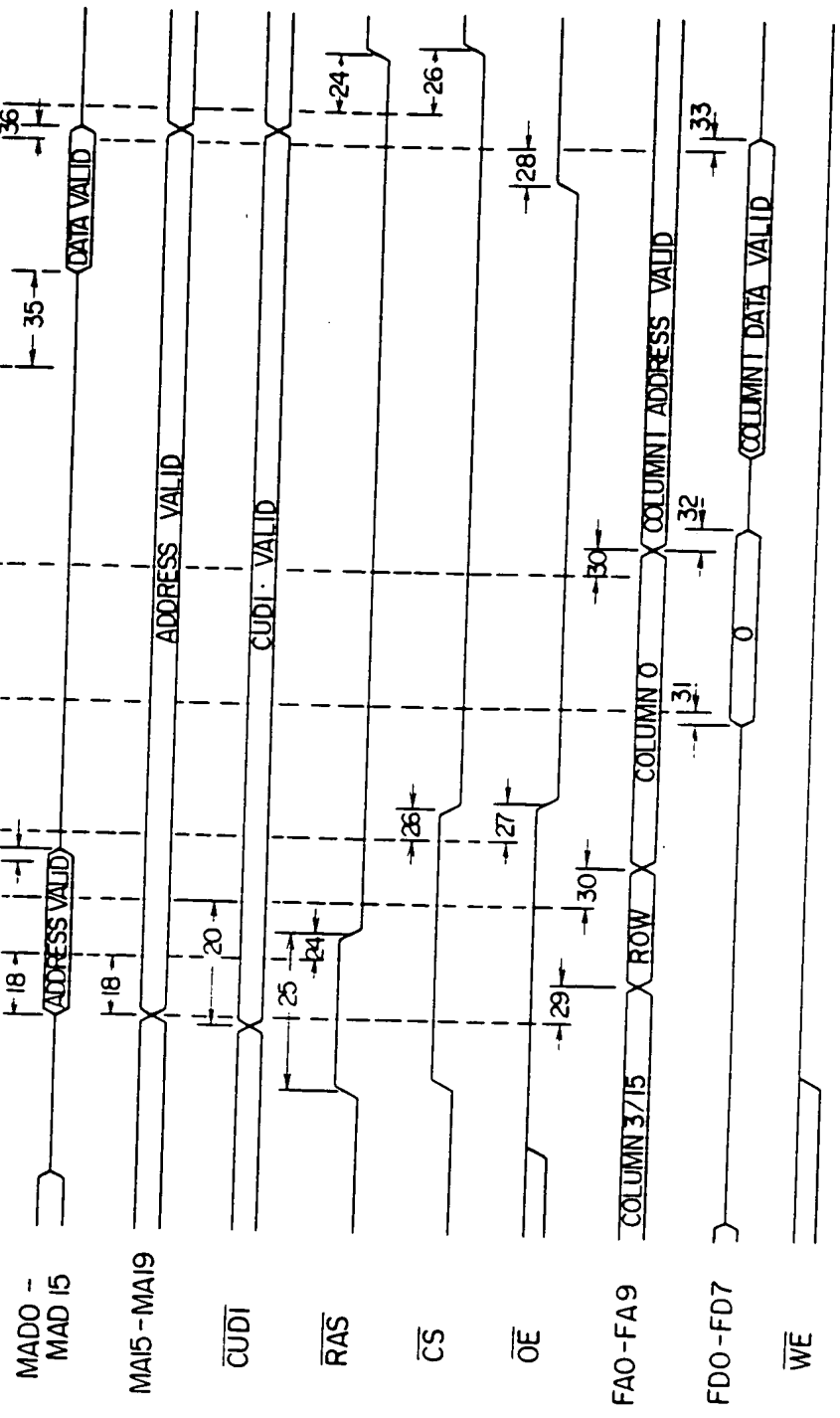

MAD0 - MAD 15
MA15 - MA19
CUDI
RAS
CS
OE
FA0 - FA9
FD0 - FD7
WE
ADDRESS VALID
DATA VALID
ADDRESS VALID
CUDI VALID
COLUMN 3715
ROW
COLUMN 0
COLUMN ADDRESS VALID
0
COLUMN DATA VALID
18
19
20
24
25
26
27
28
29
30
31
32
33
35
36

FIG 17a

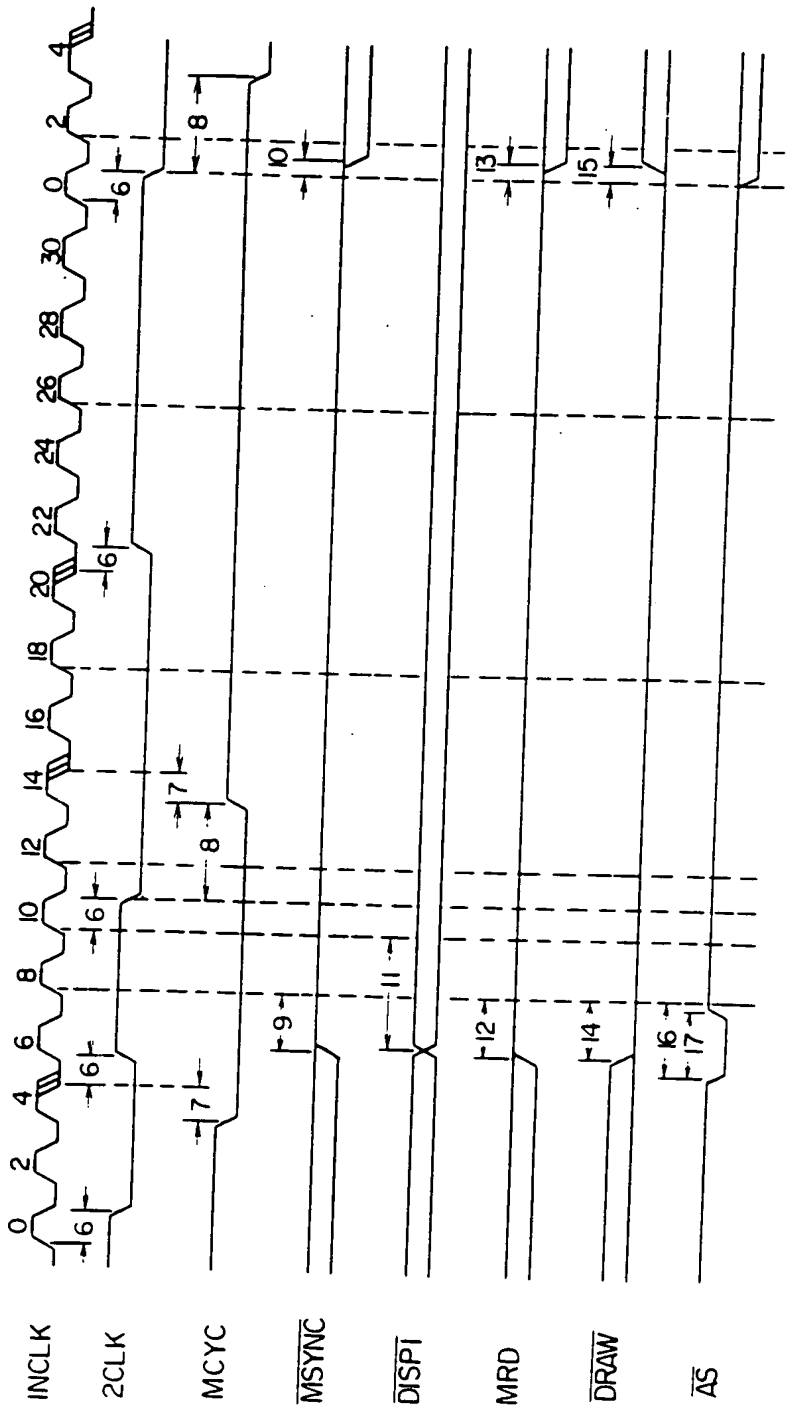


FIG. 17b

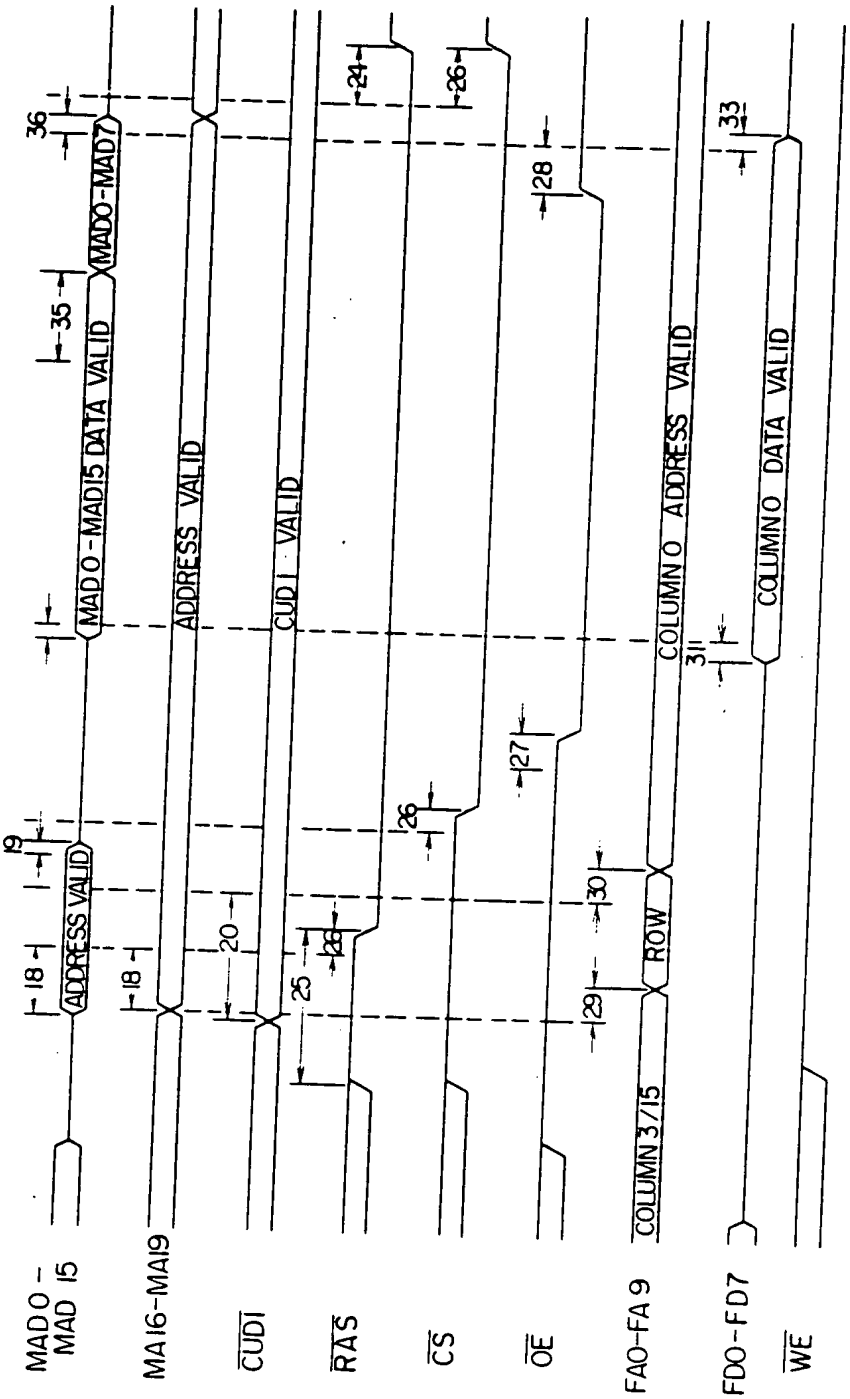

MAD0 - MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
MAD0-MAD15 DATA VALID
MAD0-MAD7
ADDRESS VALID
CUDI VALID
COLUMN 3/15
ROW
COLUMN 0 ADDRESS VALID
COLUMN 0 DATA VALID
18
19
20
25
26
27
28
29
30
31
33
35
36

FIG. 18a

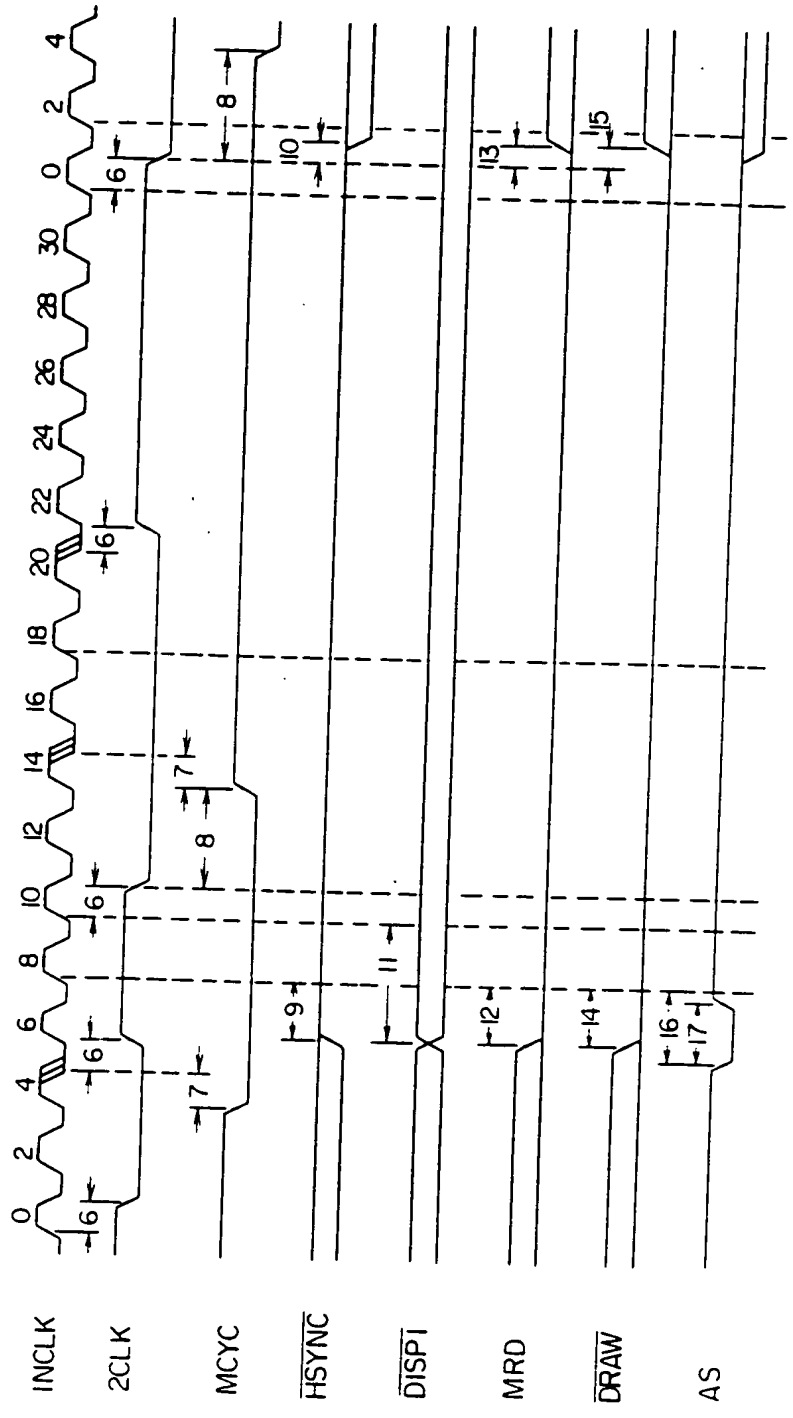


FIG. 18b

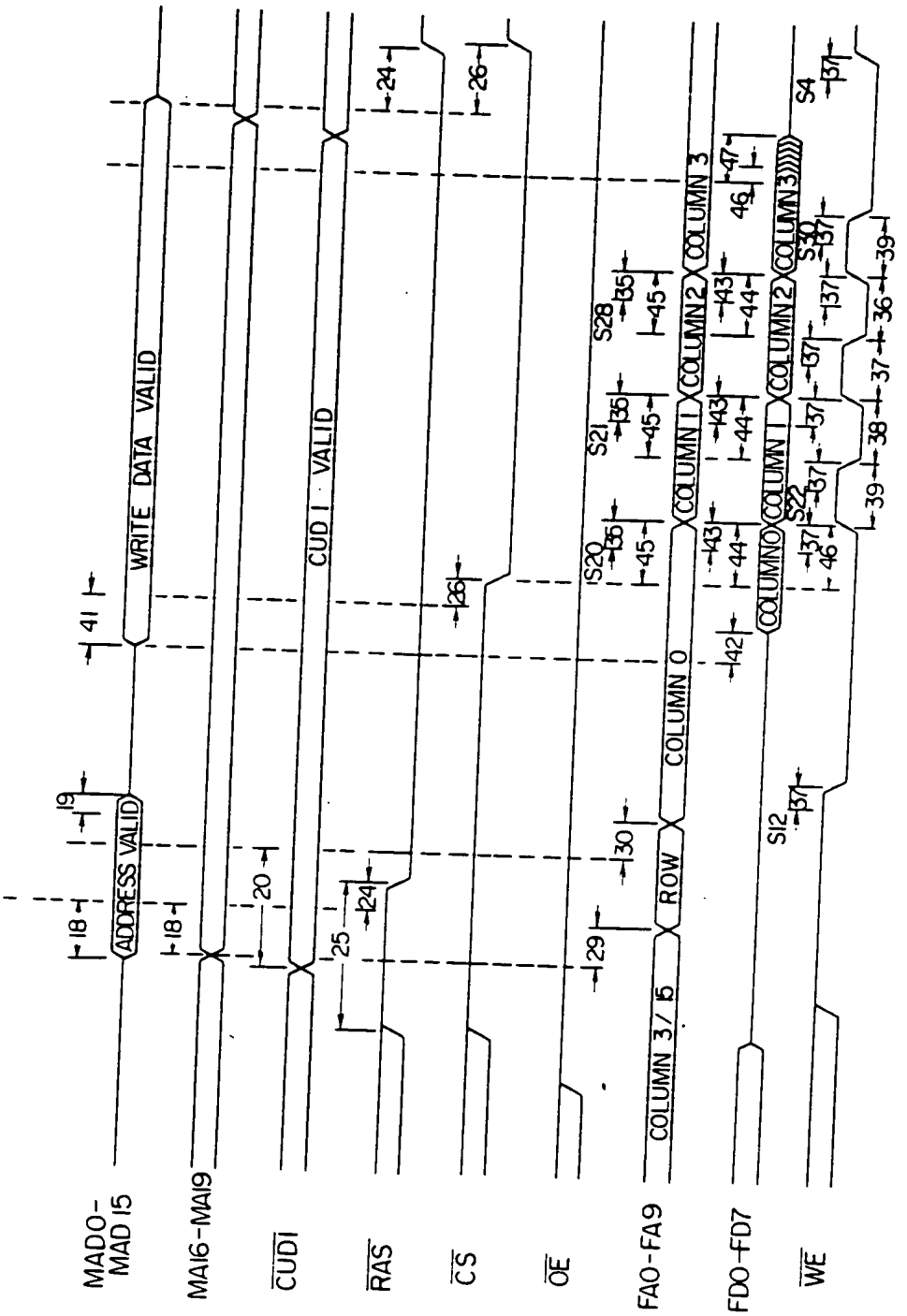

MAD0-MAD15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
WRITE DATA VALID
CUD I VALID
ROW
COLUMN 3/15
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3
18
19
41
20
24
25
26
29
30
S12
S20
S21
S22
S28
S30
S4
42
43
44
45
46
47
35
36
37
38
39

FIG. 19a

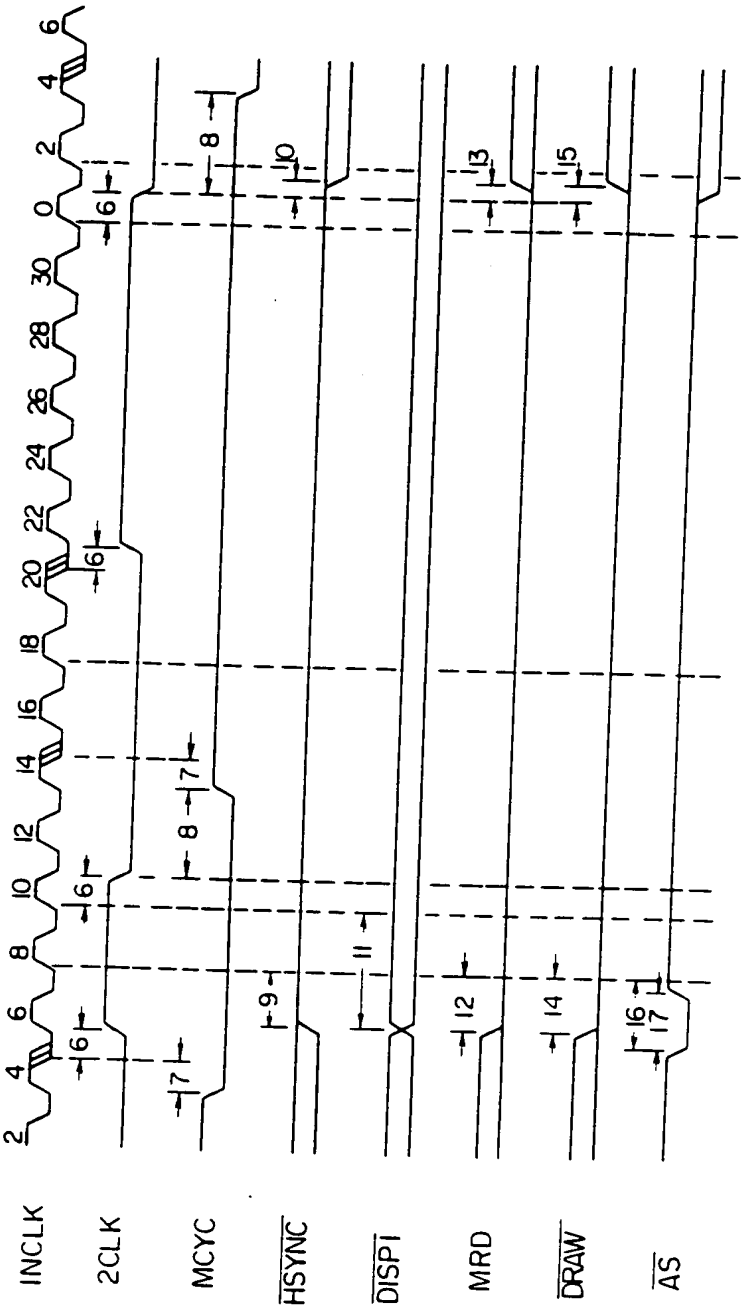


FIG. 19b

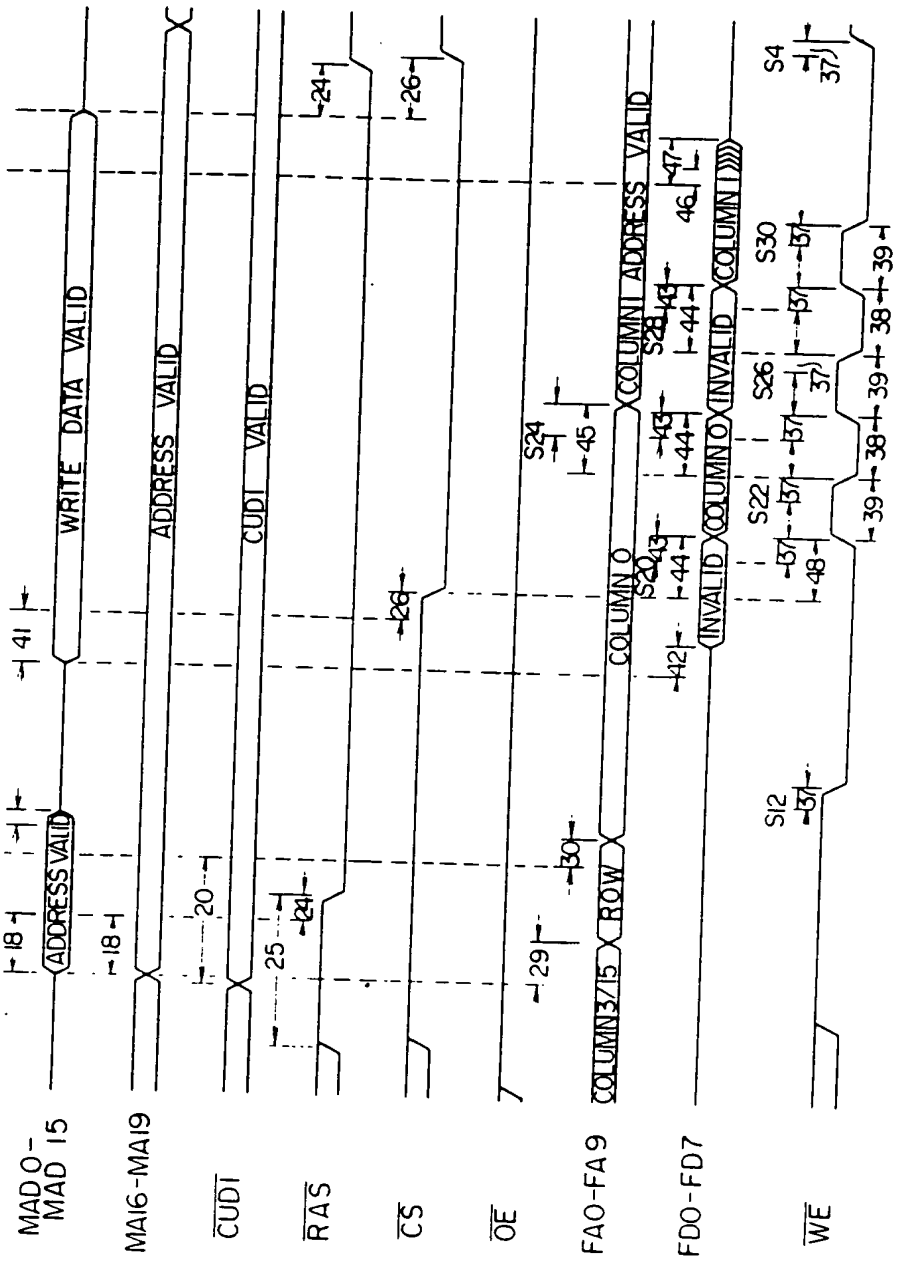

MAD 0-
MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
WRITE DATA VALID
CUDI VALID
COLUMN 0
COLUMN ADDRESS VALID
INVALID
ROW
18
19
20
21
24
25
26
29
30
41
42
43
44
45
46
47
S12
S20
S22
S24
S26
S28
S30
S4
37
38
39

FIG. 20a

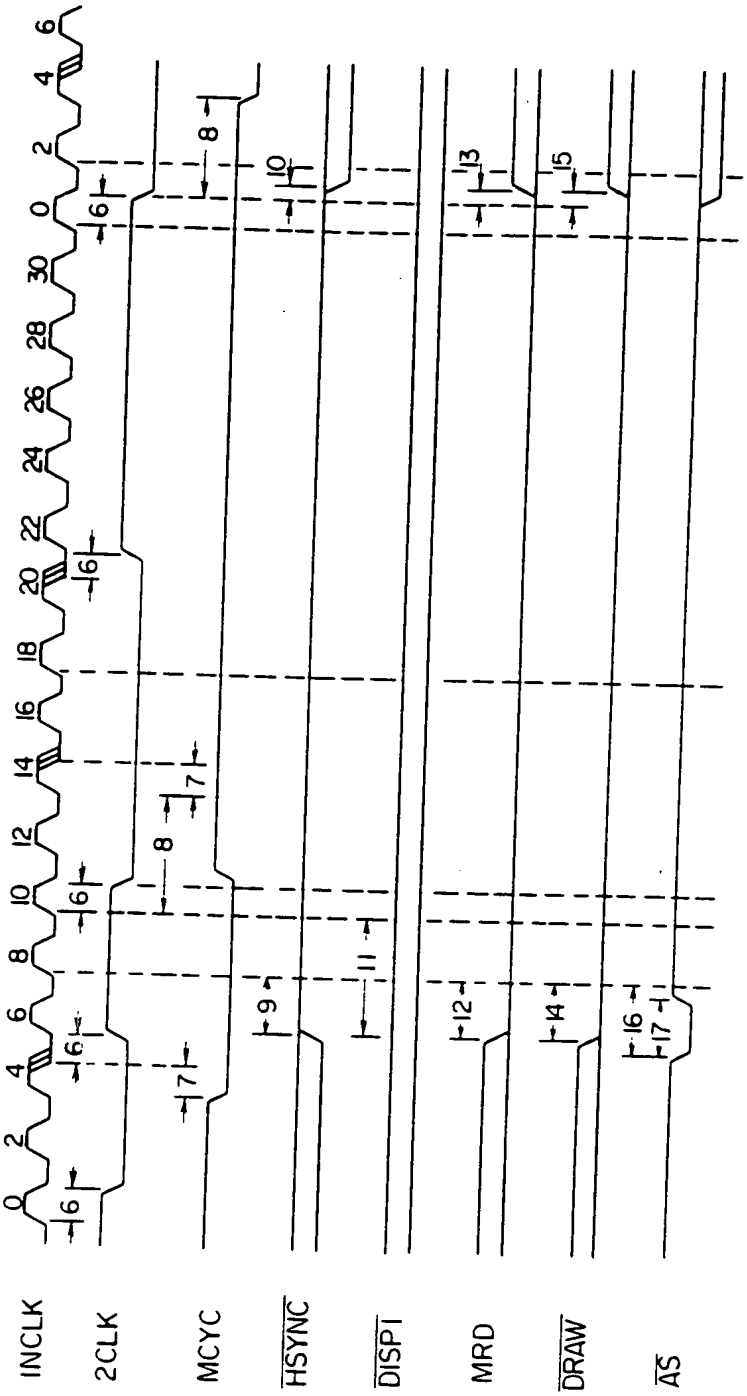

INCLK
2CLK
MCYC
HSYNC
DISPI
MRD
DRAW
AS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
0
2
4
6
6
6
6
6
6
6
7
7
8
8
8
9
10
11
12
13
14
15
16
17

FIG. 20b

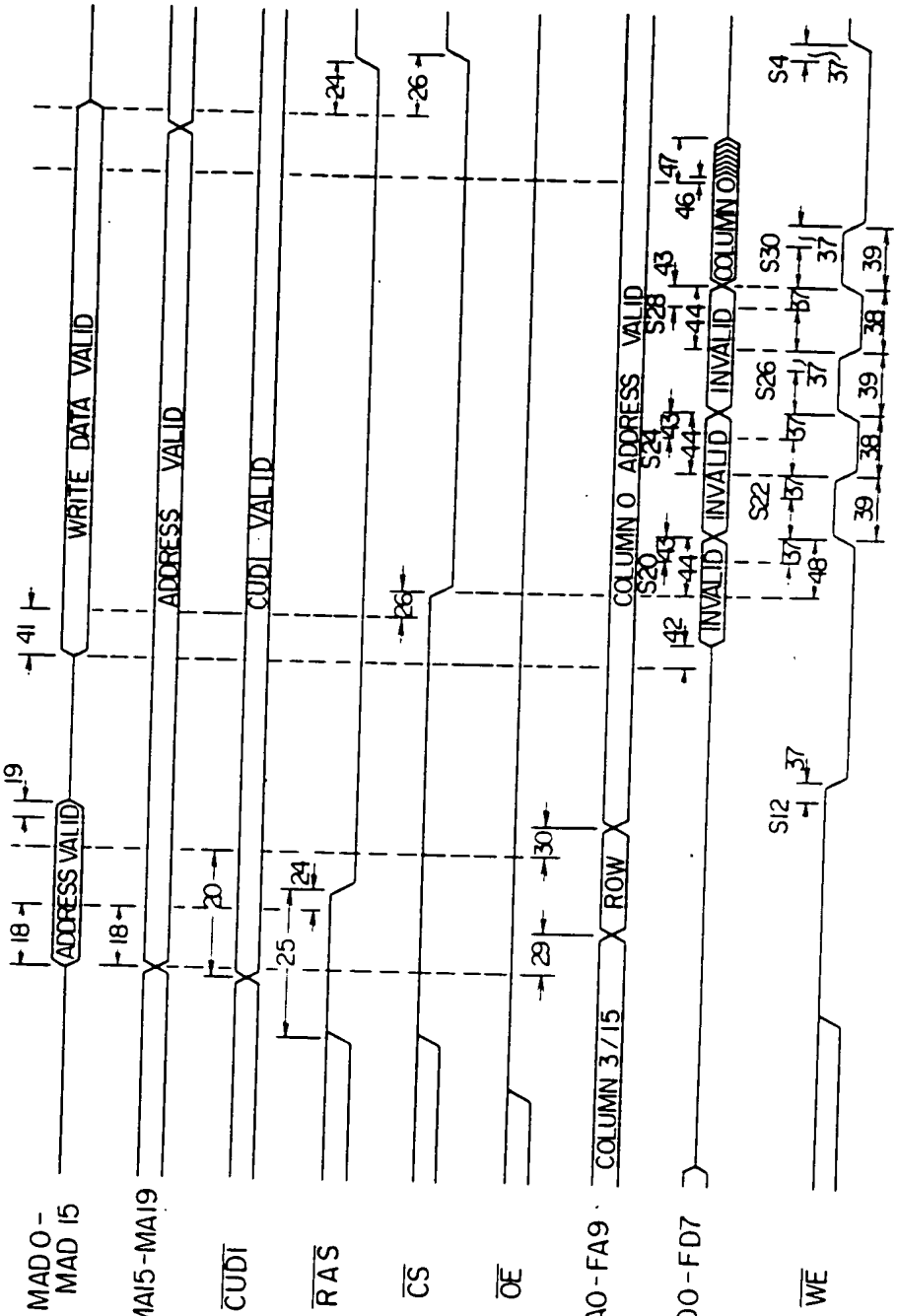

MAD0-MAD15
MA15-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
WRITE DATA VALID
ADDRESS VALID
CUDI VALID
COLUMN 3/15
ROW
COLUMN 0 ADDRESS VALID
INVALID
INVALID
INVALID
COLUMN 0
18
19
41
18
20
24
25
24
26
29
30
42
43
44
43
44
43
44
46
47
48
S12
S20
S22
S24
S26
S28
S30
S4
37
37
37
37
37
37
37
37
38
38
39
39
39

FIG 21a

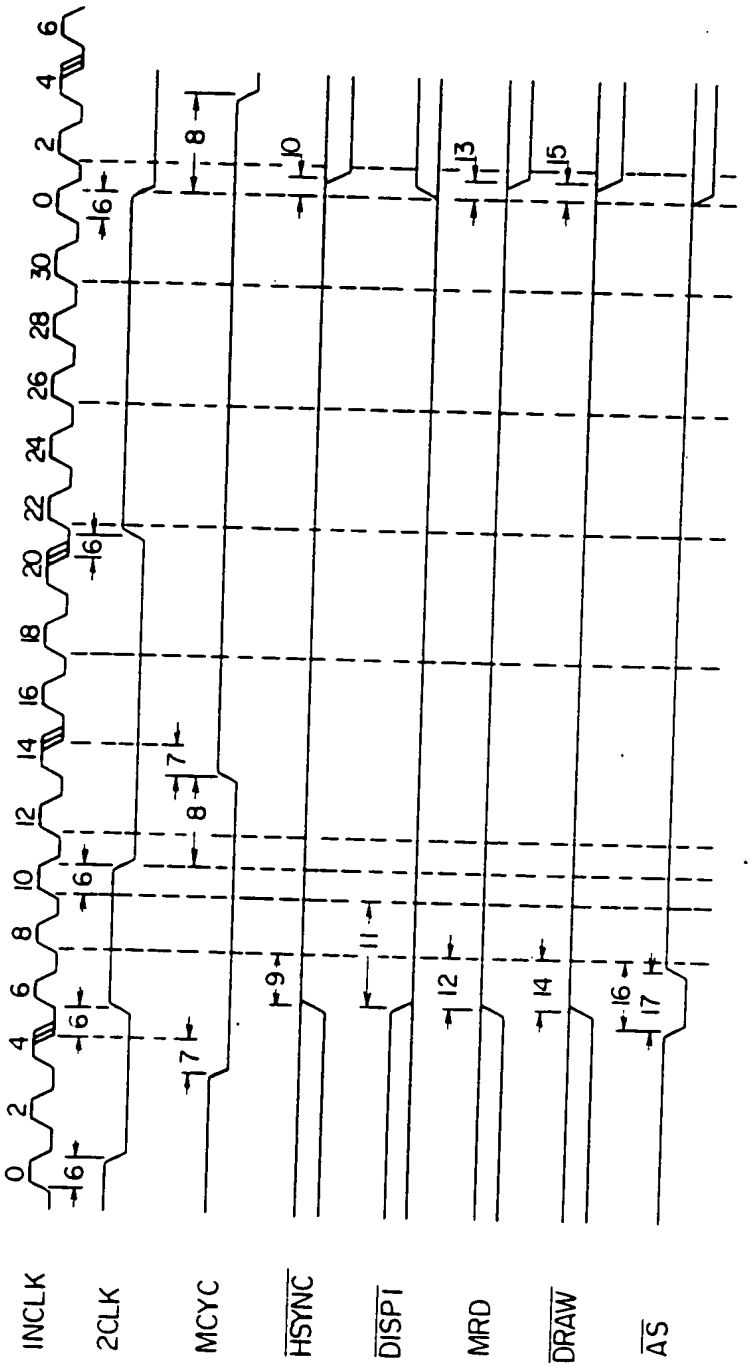


FIG. 21b

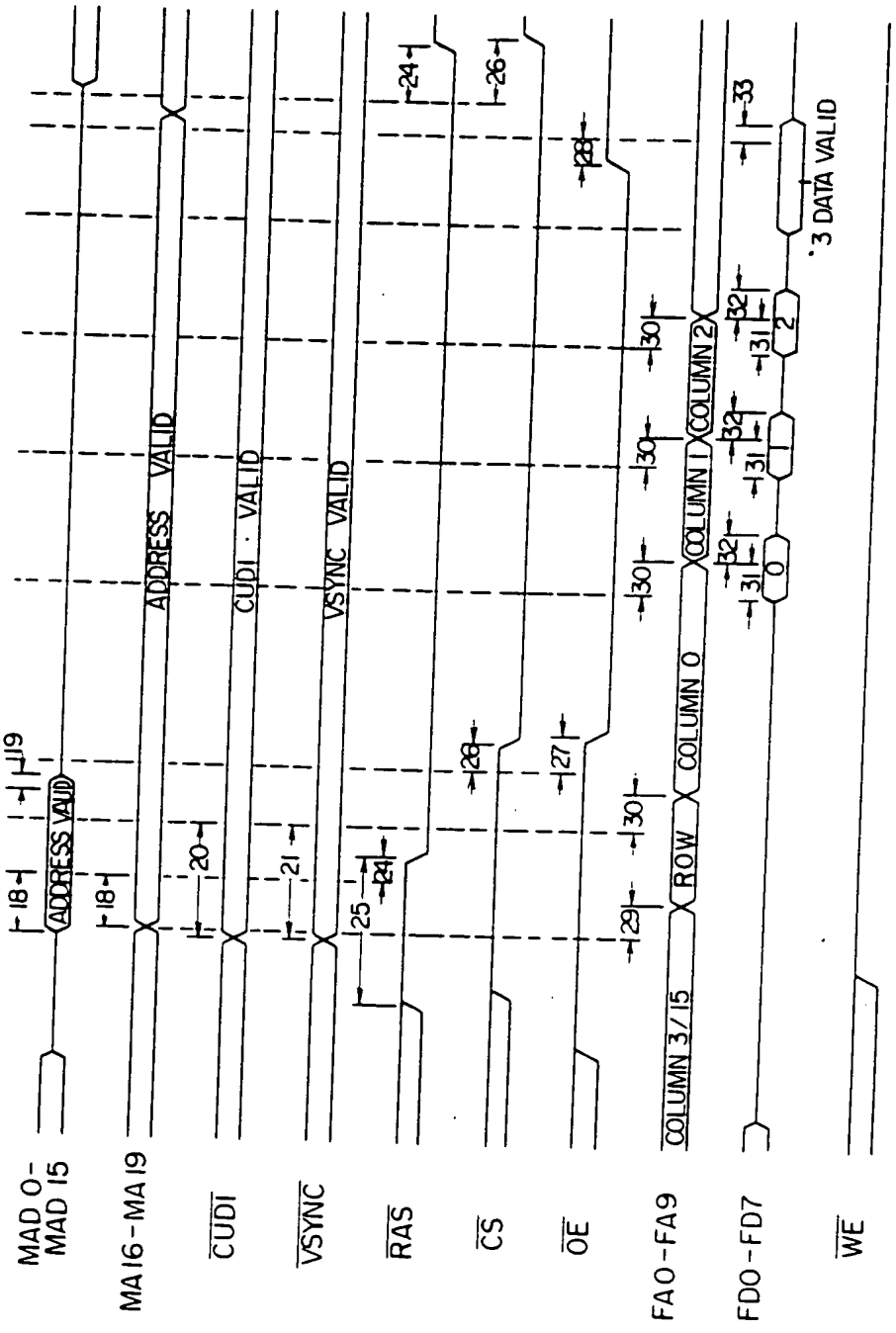

MAD 0-
MAD 15
MA16-MA19
CUDI
VSYNC
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
ADDRESS VALID
CUDI VALID
VSYNC VALID
ROW
COLUMN 3/15
COLUMN 0
COLUMN 1
COLUMN 2
3 DATA VALID
18
19
20
21
24
25
26
27
28
29
30
31
32
33

FIG. 22a

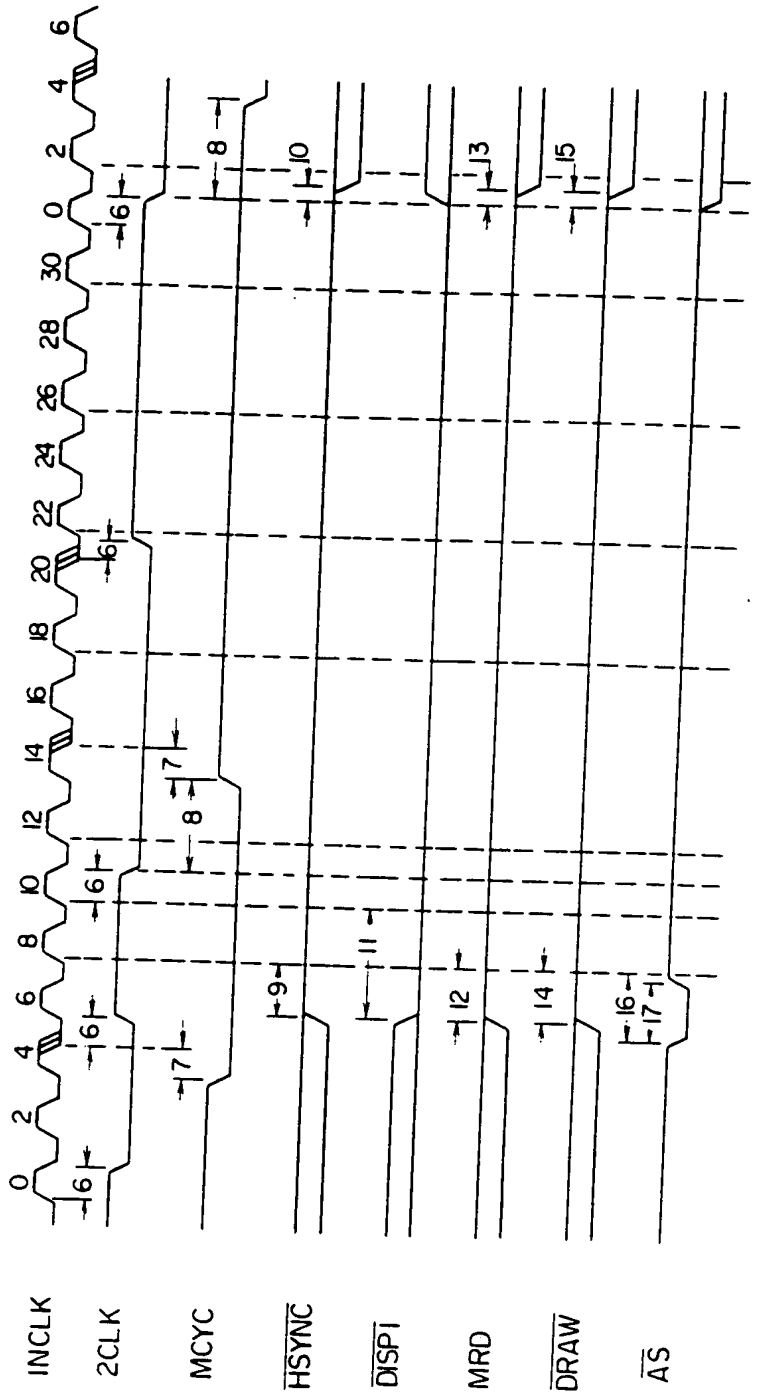


FIG. 22b

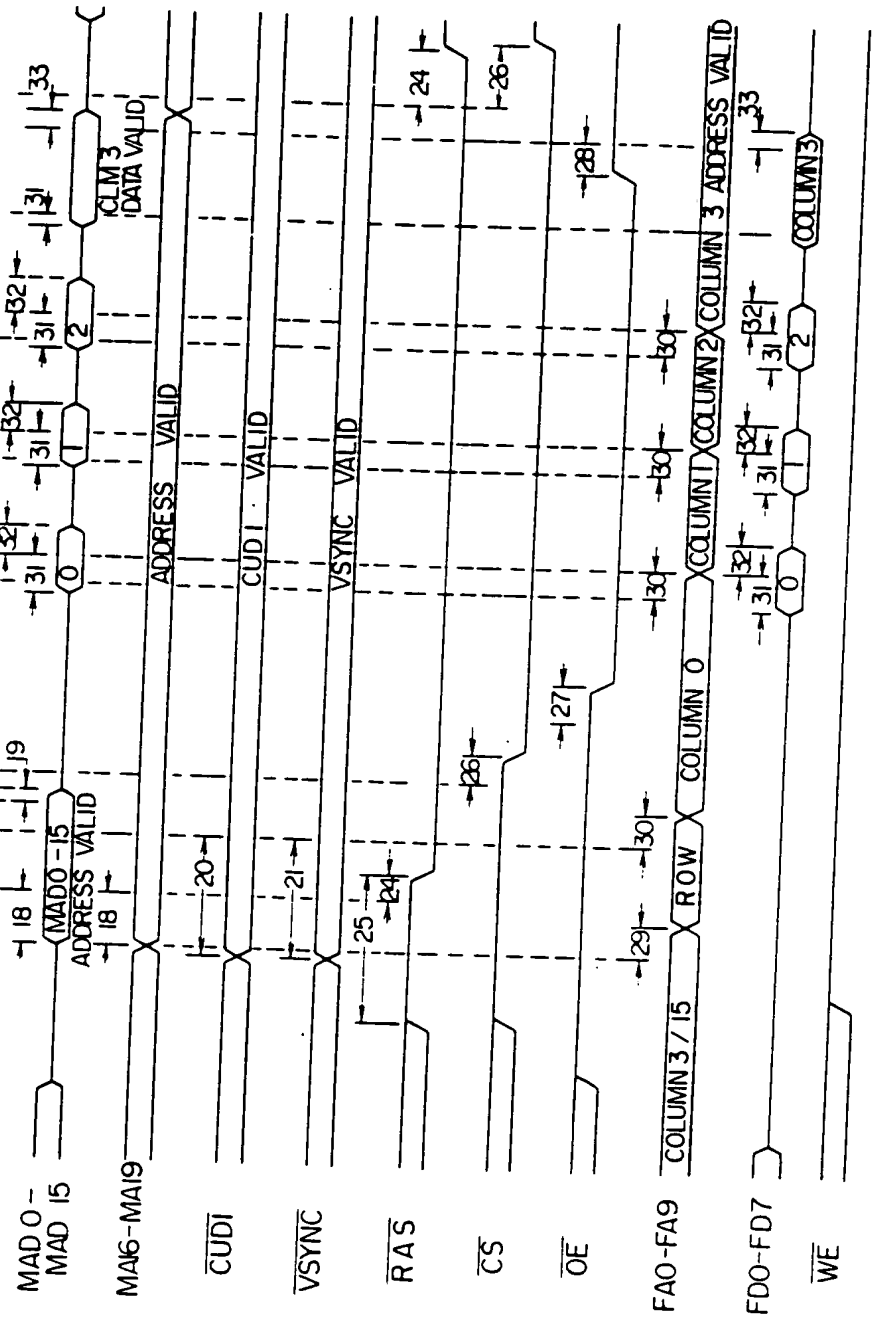

MAD 0 - MAD 15
MA6-MA19
CUDI
VSYNC
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
MAD0-15 ADDRESS VALID
ADDRESS VALID
CUDI VALID
VSYNC VALID
ROW
COLUMN 0
COLUMN 1
COLUMN 2
COLUMN 3 / 15
CLM 3 DATA VALID
COLUMN 3 ADDRESS VALID
COLUMN 3
0
1
2
18
19
20
21
24
25
26
27
28
29
30
31
32
33

FIG. 23a

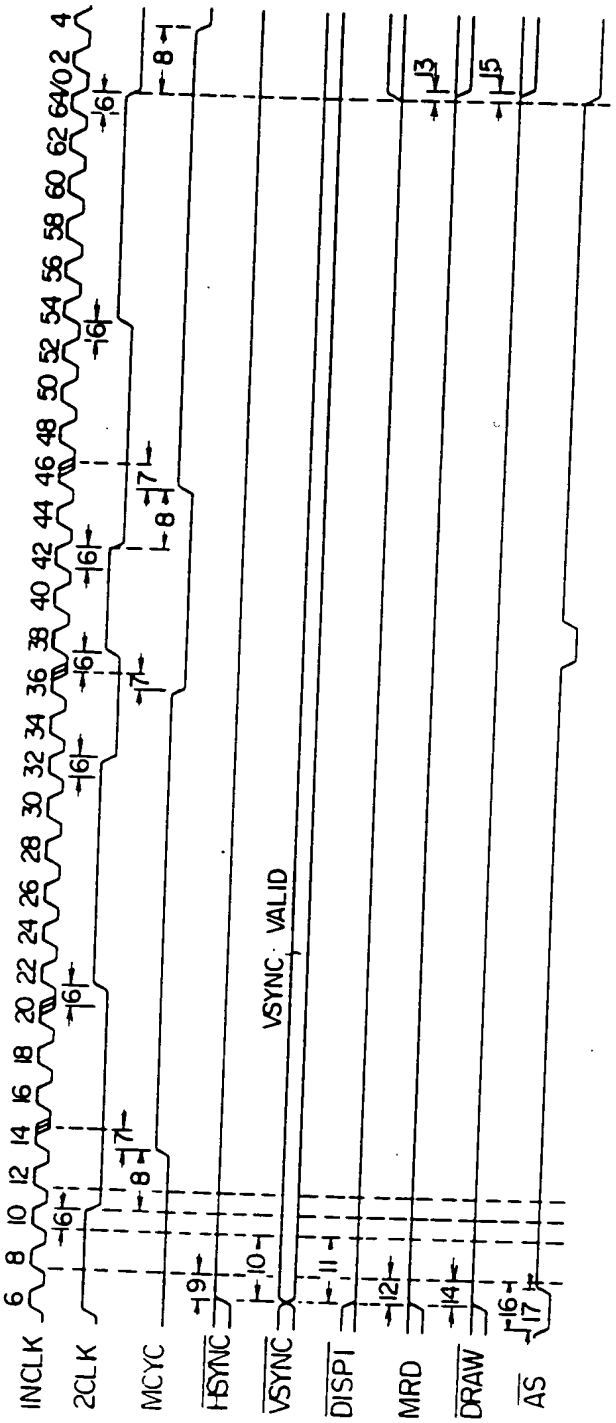


FIG. 23b

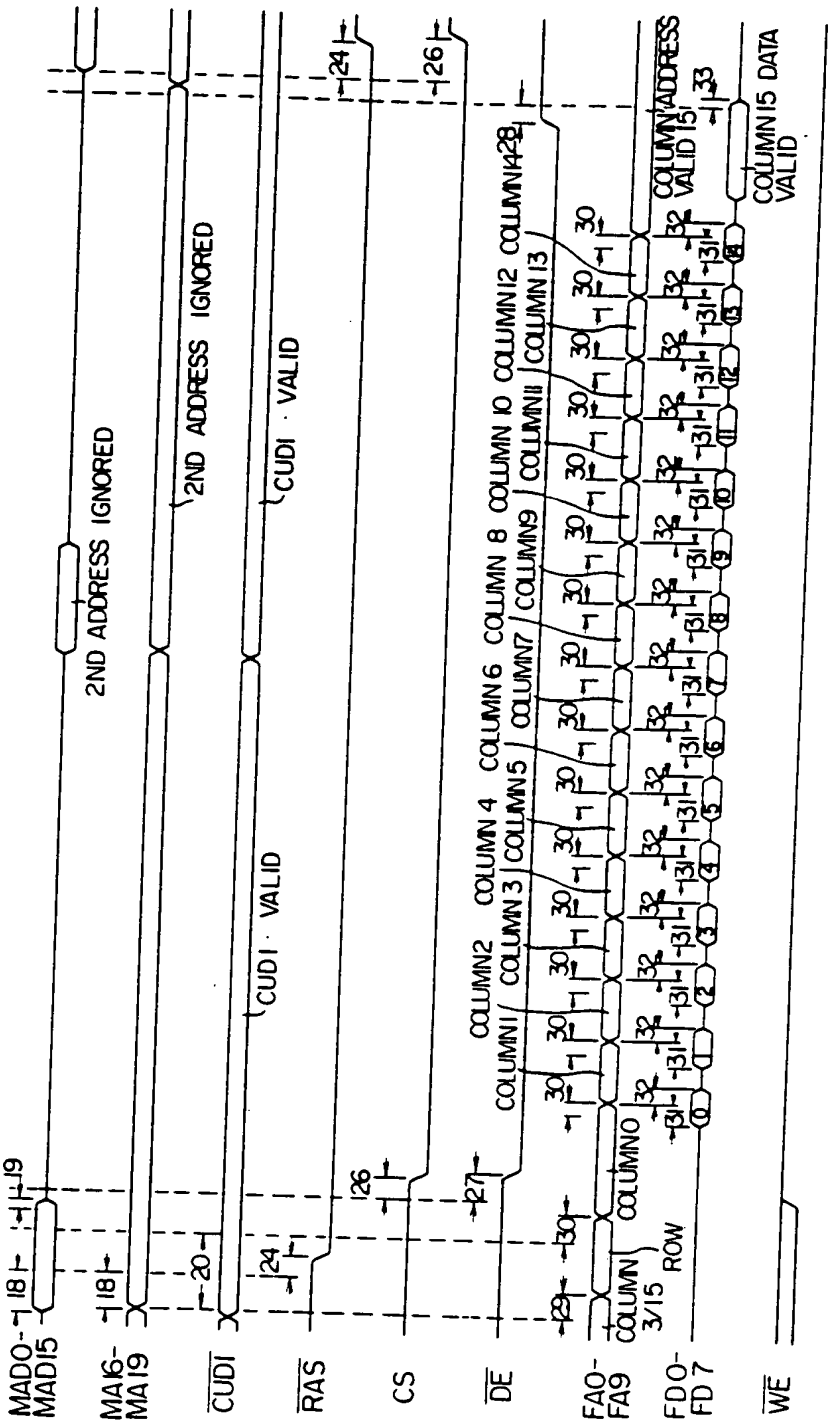

MAD0-MAD15
MA16-MA19
CUDI
RAS
CS
DE
FA0-FA9
FD0-FD7
WE
2ND ADDRESS IGNORED
2ND ADDRESS IGNORED
CUDI VALID
CUDI VALID
COLUMN2 COLUMN4 COLUMN6 COLUMN8 COLUMN10 COLUMN12 COLUMN14 28
COLUMN1/ COLUMN3 COLUMN5 COLUMN7 COLUMN9 COLUMN11 COLUMN13
COLUMN 3/15
COLUMN0
ROW
COLUMN ADDRESS VALID 15
COLUMN15 DATA VALID
18
19
20
24
26
27
30
31
32
33

FIG. 24a

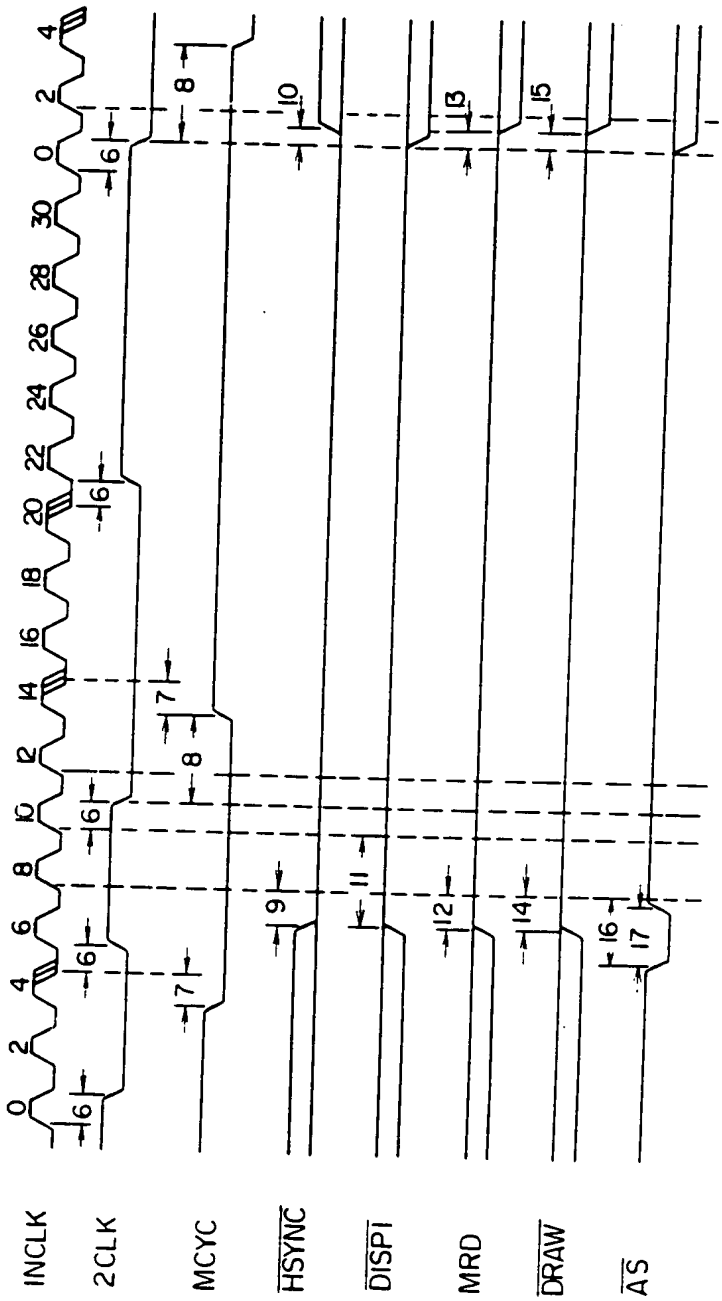


FIG 24b

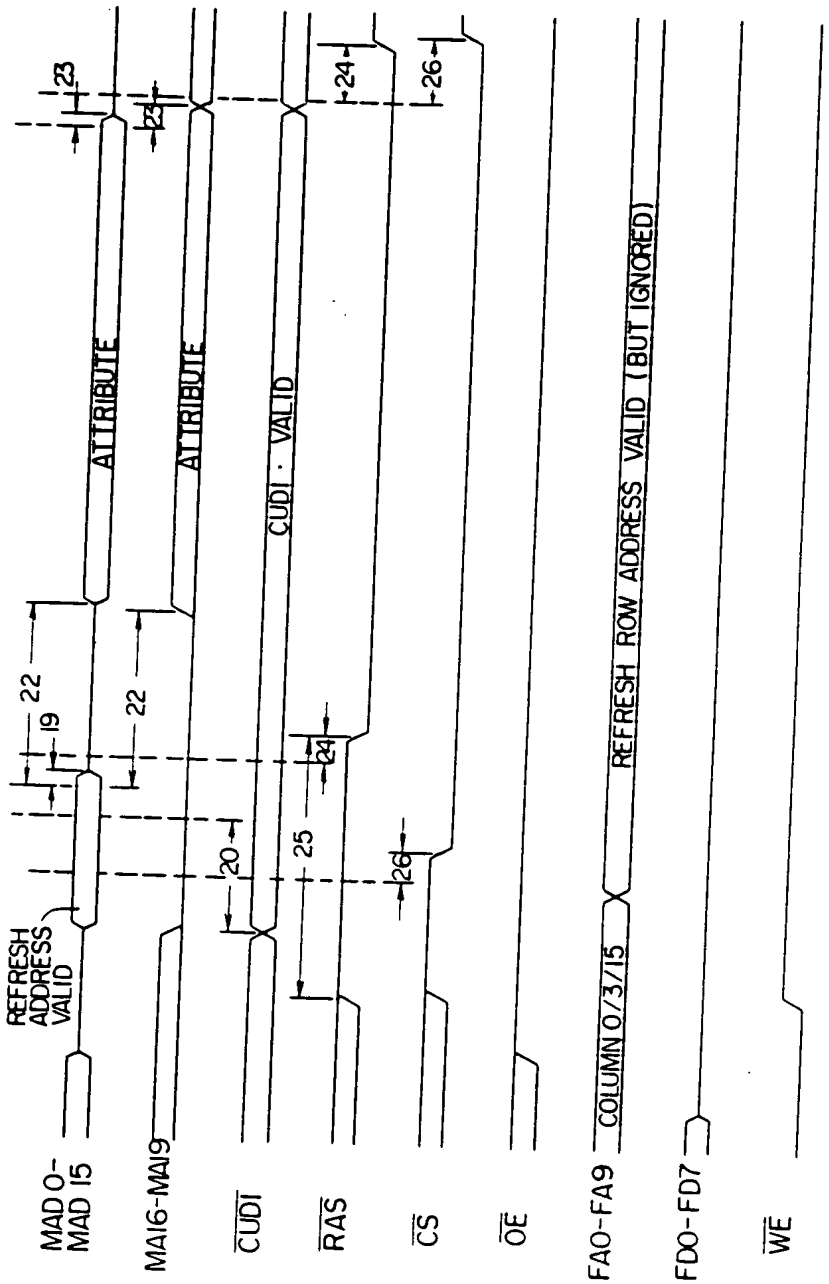

MAD 0-
MAD 15
MA16-MA19
CUDI
RAS
CS
OE
FA0-FA9
FD0-FD7
WE
REFRESH
ADDRESS
VALID
ATTRIBUTE
ATTRIBUTE
CUDI · VALID
COLUMN 0/3/15
REFRESH ROW ADDRESS VALID (BUT IGNORED)
19
20
22
22
23
23
24
24
25
26
26

FIG. 25

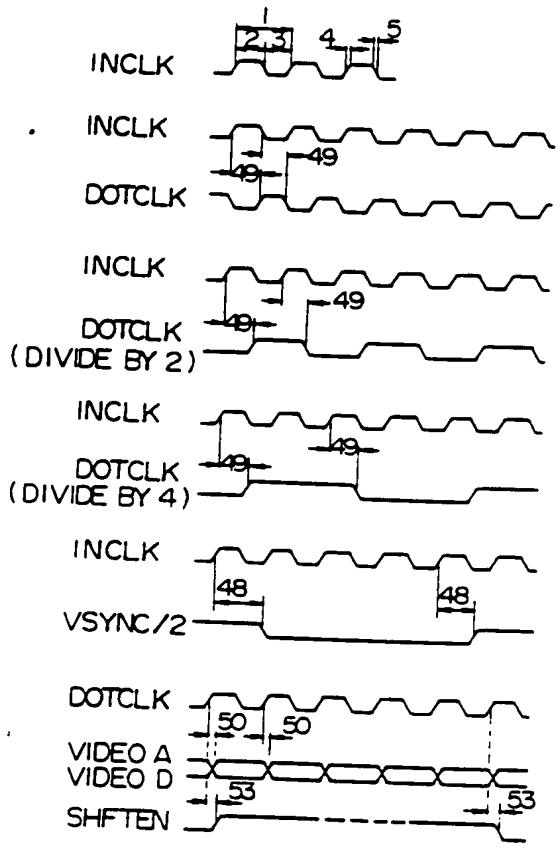
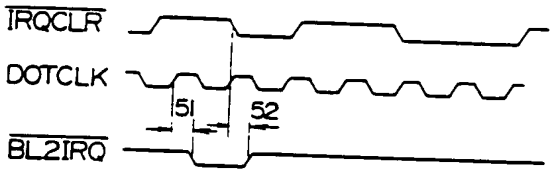

INCLK
1
2
3
4
5
INCLK
DOTCLK
49
49
INCLK
DOTCLK
(DIVIDE BY 2)
49
49
INCLK
DOTCLK
(DIVIDE BY 4)
49
49
INCLK
VSYNC/2
48
48
DOTCLK
VIDEO A
VIDEO D
SHIFTEN
50
50
53
53

FIG. 26


IRQCLR
DOTCLK
BL2IRQ
51
52

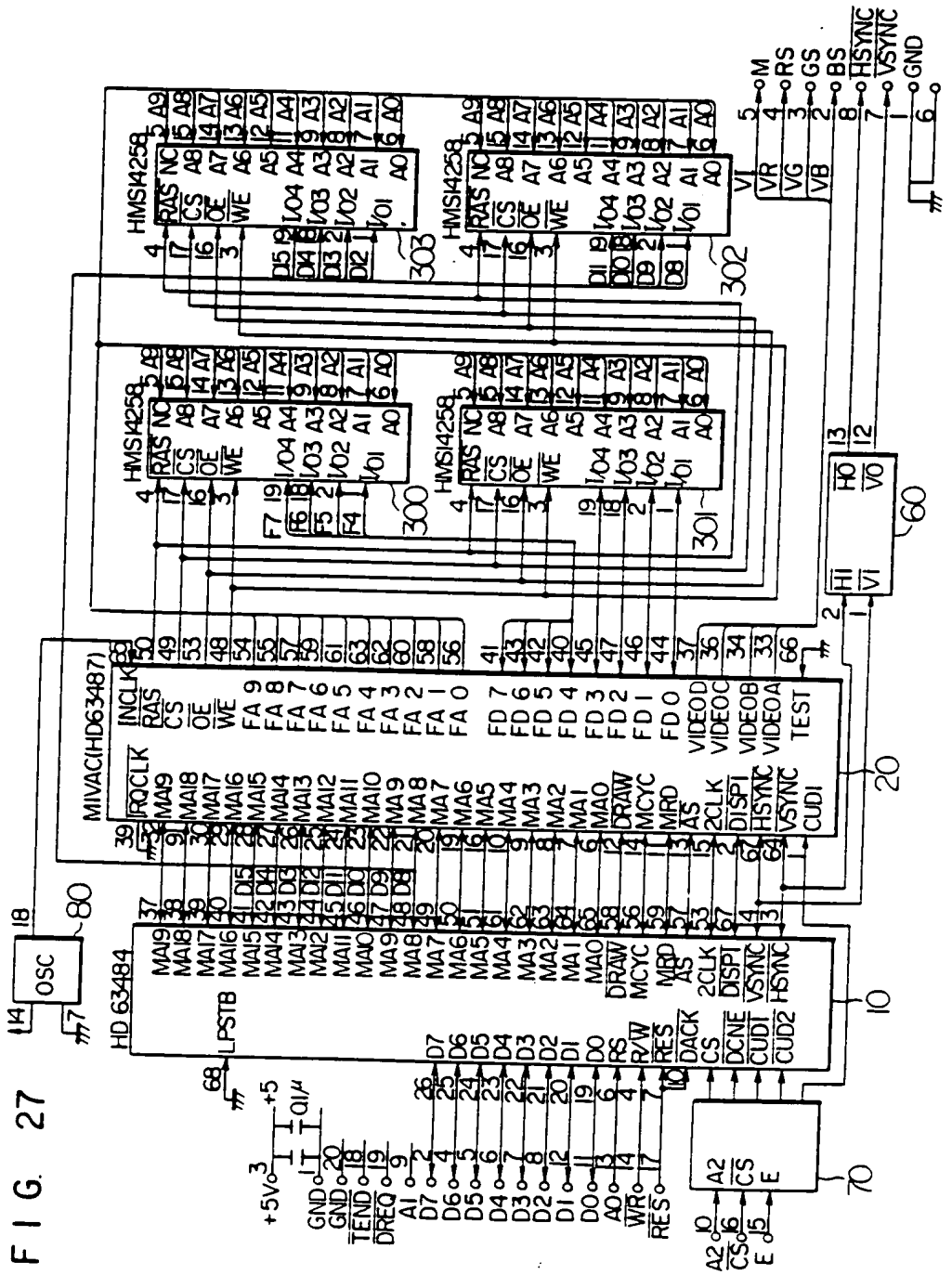

HMSI4258
MIVAC(HD63487)
HD 63484
OSC
HO
VO
M
RS
GS
BS
HSYNC
VSYNC
GND
VR
VG
VB
VI
300
301
302
303
10
20
60
70
80

FIG. 27

FIG. 28

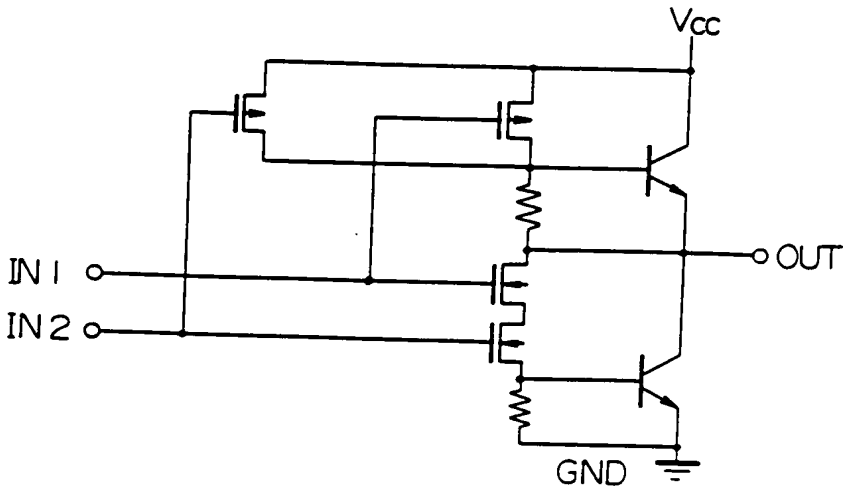


FIG. 29a

FA	4 ACCESSES / MCYC (DRAW, DISPLAY)				16 ACCESSES / 2 MCYCS (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	—	—	MAD 8	[NC0]	—	—	MAD 8	[NC0]
8	MAD 9	[NC1]	MAD 9	[NC1]	MAD 9	[NC1]	MAD 9	[NC1]
7	MAD 8	[NC2]	MA 17	MAD 7	MAD 8	[NC2]	MA 17	MAD 7
6	MAD 7	MAD 6	MA 16	MAD 6	MAD 7	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	[WC1]	MAD 11	[WC1]
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	[WC0]	MAD 10	[WC0]

[ ] : COLUMN ADDRESS COUNTER

FIG. 29b

FA	2 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)				16 ACCESSES / 2MCYCS (DISPLAY)			
	256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)		256Kx4-BIT (VMDO=0)		1Mx4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	-	-	MA 18	[NC 0]	-	-	MA 18	[NC 0]	-	-	MA 18	[NC 0]
8	MAD 9	[NC 1]	MAD 9	MAD 8	MAD 9	[NC 1]	MAD 9	MAD 8	MAD 9	[NC 1]	MAD 9	MAD 8
7	MAD 8	MAD 7	MA 17	MAD 7	MAD 8	MAD7	MA 17	MAD 7	MAD 8	MAD 7	MA 17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 14
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	[WC 2]	MAD 12	[WC 2]
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	[WC 1]	MAD 11	[WC 1]
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	[WC 0]	MAD 10	[WC 0]	MAD 10	[WC 0]	MAD 10	[WC 0]

[ ] : COLUMN ADDRESS COUNTER

FIG. 29c

FA	1 ACCESSES / MCYC (DRAW)				4 ACCESSES / MCYC (DISPLAY)			
	256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)		256K x 4-BIT (VMDO=0)		1M x 4-BIT (VMDO=1)	
	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN	ROW	COLUMN
9	–	–	MA 18	MAD 9	–	–	MA 18	MAD 9
8	MAD 9	MAD 8	MA 19	MAD 8	MAD 9	MAD 8	MA 19	MAD 8
7	MA 17	MAD 7	MA 17	MAD 7	MA 17	MAD 7	MAD17	MAD 7
6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6	MA 16	MAD 6
5	MAD 15	MAD 5	MAD15	MAD 5	MAD 15	MAD 5	MAD 15	MAD 5
4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4	MAD 14	MAD 4
3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3	MAD 13	MAD 3
2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2	MAD 12	MAD 2
1	MAD 11	MAD 1	MAD 11	MAD 1	MAD 11	WC1	MAD 11	WC 1
0	MAD 10	MAD 0	MAD 10	MAD 0	MAD 10	WC0	MAD 10	WC 0

[ ]: COLUMN ADDRESS COUNTER